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An online state-of-charge balancing strategy for energy storage STATCOM based on modular multilevel converters

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Dedico este trabalho aos meus pais.

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RESUMO

A crescente integração de fontes renováveis de energia aos sistemas elétricos tem introduzido desafios significativos relacionados à intermitência e à estabilidade da rede. Nesse contexto, o Compensador Síncrono Estático com Armazenamento de Energia (ES-STATCOM, do inglês *Energy Storage Static Synchronous Compensator*), baseado na topologia do Conversor Multinível Modular, surge como uma solução eficaz para aumentar a flexibilidade e a confiabilidade do sistema elétrico. No entanto, a configuração na qual os *racks* de baterias são conectados nesses sistemas, associada às variadas condições operacionais, pode causar desequilíbrios no estado de carga (SoC, do inglês *State of Charge*) entre os módulos de baterias, reduzindo a eficiência e a vida útil do sistema caso ele seja operado sob essas condições. Para mitigar esse problema, a presente dissertação propõe uma estratégia de balanceamento *online* do SoC, empregando um algoritmo integrado à estrutura de controle do ES-STATCOM. Adicionalmente, foram projetadas malhas de controle da corrente de saída e de supressão de correntes circulantes no referencial síncrono *dq*. A abordagem desenvolvida permite a realização do balanceamento do SoC, mantendo simultaneamente a capacidade do conversor de injetar e absorver potências ativa e reativa instantâneas. Essa estratégia não apenas melhora a utilização do Sistema de Armazenamento de Energia em Baterias (BESS, do inglês *Battery Energy Storage System*), como também aumenta a confiabilidade operacional do ES-STATCOM sob diferentes condições da rede elétrica. A metodologia proposta foi verificada por meio de simulações detalhadas no *software* PSCAD/EMTDC, nas quais um ES-STATCOM com 18 submódulos por braço, conectado a um BESS em configuração distribuída de estágio único, utilizando células de bateria de primeira vida de íon-lítio nos *racks* de baterias, foi modelado e conectado a um sistema trifásico equilibrado com nível de tensão de 13,8 kV. As dinâmicas do ES-STATCOM durante o balanceamento do SoC foram analisadas em diferentes cenários, injetando e absorvendo potências ativa e reativa em seus terminais. Posteriormente, o ES-STATCOM foi testado em um sistema IEEE 14-barras modificado, a fim de avaliar seu desempenho durante o suporte de frequência e tensão, respectivamente, após a conexão de uma grande carga e a aplicação de uma falta simétrica na rede. Os resultados da simulação confirmaram a efetividade da estratégia de controle proposta e sua capacidade de manter o balanceamento do SoC enquanto o conversor presta serviços auxiliares à rede elétrica.

Palavras-chave: Conversor Multinível Modular. ES-STATCOM. Algoritmo de Balanceamento de SoC.

ABSTRACT

The increasing integration of renewable energy sources into power systems has introduced significant challenges related to intermittency and grid stability. In this context, the Energy Storage Static Synchronous Compensator (ES-STATCOM), based on the Modular Multilevel Converter topology, emerges as an effective solution to enhance the flexibility and reliability of power systems. However, the configuration in which battery racks are connected in these systems, combined with varying operating conditions, can cause State of Charge (SoC) imbalances among battery modules, reducing both the system's efficiency and its lifetime if operated under such conditions. To address this issue, this dissertation proposes an online SoC balancing strategy employing an algorithm integrated into the ES-STATCOM control structure. In addition, control loops for output current regulation and circulating current suppression were designed in the synchronous dq reference frame. The developed approach enables the SoC balancing process while simultaneously maintaining the converter's capability to inject and absorb active and reactive instantaneous power. This strategy not only improves the utilization of the Battery Energy Storage System (BESS) but also enhances the operational reliability of the ES-STATCOM under different grid conditions. The proposed methodology was verified through detailed simulations using the PSCAD/EMTDC software, where an ES-STATCOM with 18 sub-modules per arm, connected to a BESS in a single-stage distributed configuration with first-life lithium-ion battery cells installed in the racks, was modeled and connected to a balanced three-phase system with a voltage level of 13.8 kV. The ES-STATCOM dynamics during the SoC balancing process were analyzed in different scenarios, injecting and absorbing active and reactive power at its terminals. Subsequently, the ES-STATCOM was tested in a modified IEEE 14-bus system to evaluate its performance during frequency and voltage support, respectively, after the connection of a large load and the occurrence of a symmetrical fault. The simulation results confirmed the effectiveness of the proposed control strategy and its ability to maintain SoC balancing while providing ancillary services to the power grid.

Keywords: Modular Multilevel Converter. ES-STATCOM. SoC Balancing Algorithm.

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LIST OF ABBREVIATIONS AND ACRONYMS

ac	alternating current
APOD-PWM	Alternate Phase Opposition Disposition PWM Carrier
BESS	Battery Energy Storage Systems
BMS	Battery Management System
CCSC	Circulating Current Suppressing Control
dc	direct current
DS	Double-Star
DSOGI	Double Second Order Generalized Integrator
EMS	Energy Management System
EP	Electrical Performance
ESS	Energy Storage Systems
ES-STATCOM	Energy Storage Static Synchronous Compensator
FBSM	Full-bridge Submodule
HBSM	Half-bridge Submodule
IEA	International Energy Agency
IGBT	Insulated Gate Bipolar Transistor
LS-PWM	Level-shifted PWM Carrier
MMC	Modular Multilevel Converter
NPC	Neutral Point Clamped
PCC	Point of Common Coupling
PCS	Power Conversion System
PD-PWM	Phase Disposition PWM Carrier
PI	proporcional-integral
PLL	Phase-Locked Loop
POD-PWM	Phase Opposition Disposition PWM Carrier
PS-PWM	Phase-shifted PWM Carrier
PWM	Pulse Width Modulation
PV	photovoltaic
RES	Renewable Energy Sources
RMS	root mean square

SCiB	Super Charge ion Battery
SM	submodule
SRF	Synchronous Reference Frame
STATCOM	Static Synchronous Compensator
THD	Total Harmonic Distortion
USA	United States of America
UPS	Uninterruptible Power Supply
VSC	Voltage Source Converter
SoC	state of charge
SoH	state of health

LIST OF SYMBOLS

B System damping

C Capacitance of the SM

C_{bat} Nominal capacity of the battery unit

$C_{bat,n}$ Nominal capacity of the battery rack

C_{rate} Discharge rate of the battery unit

$C_{rate,n}$ Recommended discharge rate factor

$(_{dq})$ Subscript that denotes the direct and quadrature coordinates in the SRF

E Requirement of the ES-STATCOM energy storage

$E_{bat,n}$ Nominal energy of a single battery pack

e_{bat} Non-load voltage of the battery rack

i_{bat} Instantaneous battery current

i_{Cap} Instantaneous capacitor current

$i_{circ,k}$ Instantaneous circulating currents through de phase k arm

$i_{s,k}$ Instantaneous output current of the ES-STATCOM in phase k

$i_{u,k}$ Instantaneous current of the upper arm in phase k

$i_{w,k}$ Instantaneous current of the lower arm in phase k

J Moment of inertia of the generation system

(j) Superscript and/or subscript that denotes the upper(u) or lower(w) arm of the ES-STATCOM

$(_k)$ Subscript that denotes the phases a, b, and c of the three-phase system

$k_{circ,i}$ Integral gain of the circulating current suppressing control loop

$k_{circ,p}$ Proportional gain of the circulating current suppressing control loop

$k_{i,cs}$ Integral gain of the output current control loop

$k_{i,\omega}$ Integral gain of the frequency support control loop

$k_{i,SoC_{avg}}$ Integral gain of the SoC global control loop

$k_{i,V_{pcc}}$ Integral gain of the voltage support control loop

$k_{p,cs}$ Proportional gain of the output current control loop

$k_{p,\omega}$ Proportional gain of the frequency support control loop

$k_{p,SoC_{avg}}$ Proportional gain of the SoC global control loop

$k_{p,V_{pcc}}$ Proportional gain of the voltage support control loop

L Inductance of the first-order filter at the converter's output

L_{arm} Inductance of the ES-STATCOM arm

L_{eq} Equivalent inductance of the converter's system

$m_{j,k}$ Modulation index for the upper or lower SM in phase k

m_{max} Maximum modulation index

$m_{s,x}$ Modulation index of the terminal voltage in the dq coordinates ($_x$)

$m_{s,k}$ Modulation index of the terminal voltage in phase k

$m_{tm,k}$ Modulation index due to the voltage imbalance in phase k

N Number of SM in each arm of the ES-STATCOM

N_p Battery packs connected in parallel

N_s Battery packs connected in series

n_{cells} Number of cells in the battery pack

$P_{bat,n_{min}}$ Minimum power available from each battery pack

$P_{bat,rack_{min}}$ Minimum power available from each battery rack

P_{mec} Mechanical power of the generation system

$P_{mec,pu}$ Mechanical power of the generation system in per-unit

p_s^* Instantaneous active power reference set for the ES-STATCOM

p_s Instantaneous active power at the terminals of the ES-STATCOM

p_k Instantaneous active power flowing through the leg k

q_s^* Instantaneous reactive power reference set for the ES-STATCOM

q_s Instantaneous reactive power at the terminals of the ES-STATCOM

R Resistance of the first-order filter at the converter's output

R_{arm} Resistance of the ES-STATCOM arm

R_{bat} Battery's internal resistance

R_{eq} Equivalent resistance of the converter's system

S Rated apparent power of the ES-STATCOM

S_1 Top IGBT

S_2 Bottom IGBT

SoC Instantaneous SoC estimation

SoC_0 Initial value of the SoC

$SoC_{0,pu}$ Per-unit initial value of the SoC

$SoC_{avg,k}$ Average SoC value in phase k

$SoC^j_{k,n}$ Instantaneous n^{th} SoC of the upper or lower SM in phase k

SoC_{max} Maximum allowable SoC value

SoC_{min} Minimum allowable SoC value

SoC_{pu} Instantaneous SoC estimation in per-unit

v_C Instantaneous voltage of the capacitor within the SM

v_{bat} Instantaneous output voltage of the Battery rack

$v_{bat,max}$ Maximum voltage of a single battery pack

$v_{bat,min}$ Minimum voltage of a single battery pack

$v_{pcc,k}$ Instantaneous voltage at the PCC in phase k

v_{SM} Instantaneous terminal voltage of the SM

$v_{t,k}$ Instantaneous terminal voltage of the ES-STATCOM in phase k

$v_{tm,k}$ Instantaneous voltage imbalance for each ES-STATCOM leg

$v_{u,k}$ Instantaneous voltage of the upper arm in phase k

$v_{w,k}$ Instantaneous voltage of the lower arm in phase k

V_{dc} dc-link voltage of the ES-STATCOM

$V_{dc,min}$ Minimum value of the dc-link of the ES-STATCOM

X_{arm} Per-unit arm reactance

X_{eq} Per-unit equivalent reactance of the ES-STATCOM

$(_x)$ Subscript that denotes the coordinates d and q

Z Impedance at the converter's output

ω Angular frequency at the PCC

θ Phase angle at the PCC

f Nominal grid frequency

f_{samp} Sampling frequency

f_{sw} Switching frequency

f_{sw} Per-unit reactance on the grid-side

$(^*)$ Superscript that denotes reference value

$(_1)$ Subscript that denotes positive sequence

$(_2)$ Subscript that denotes negative sequence

CONTENTS

1 INTRODUCTION

1.1 CONTEXT AND RELEVANCE

Climate change is one of the greatest challenges of the 21st century, demanding profound transformations in energy production and consumption systems. In this context, the adoption of Renewable Energy Sources (RES) for electricity generation, heating in buildings, industrial processes and transportation systems has become a key technology for limiting the average global temperature rise to below 1.5°C (IEA, 2025).

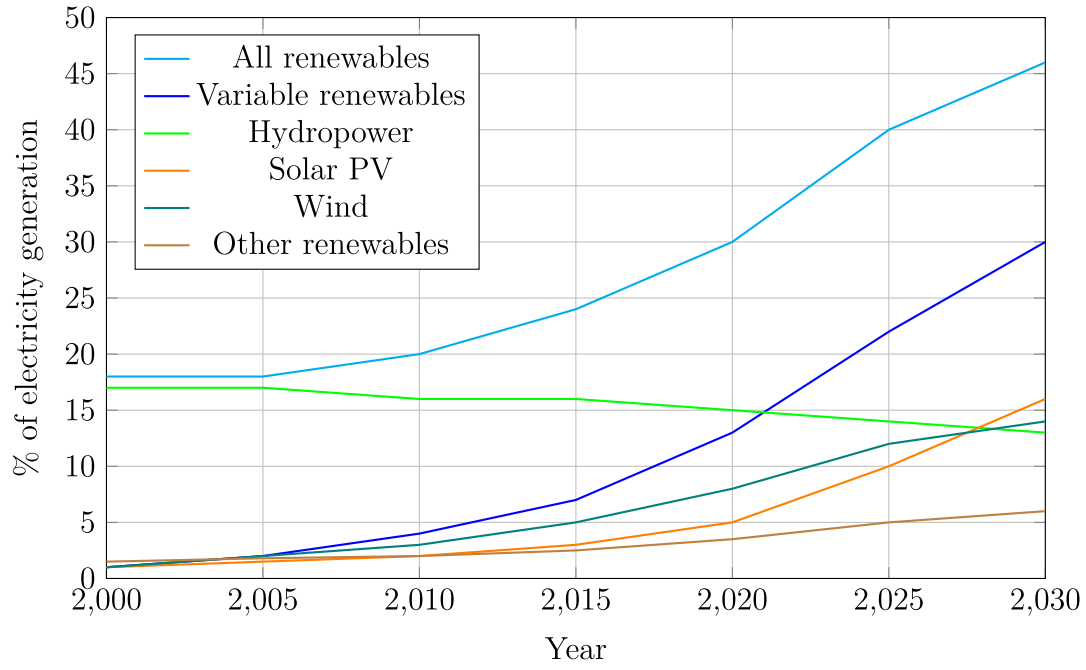
According to the International Energy Agency (IEA), global electricity generation from renewable sources is projected to exceed 17,000 TWh by the end of this decade, representing an increase of nearly 90% compared to the levels recorded in 2023. This amount would be sufficient to meet, combined, the entire electricity demand of China and the United States of America (USA) in 2030, the two largest economies and also the biggest energy consumers in the world. This scenario highlights the accelerating pace of the global energy transition and the increasingly strategic role of renewable sources in meeting global energy demand.

Figure 1 shows the share of electricity generation from renewable sources by technology, from 2000 to 2030. In this figure, the light green represents hydropower generation, dark green and orange represent, respectively, wind and solar photovoltaic (PV) generation, and indigo blue represents variable renewables, which is the sum of solar, wind, and other renewables. In the next five years, several renewable energy milestones are expected to be reached. Note that by 2027, wind and PV power generation are projected to match hydropower generation. By 2029, solar PV electricity generation is expected to surpass hydropower, making it the largest RES worldwide, with wind power generation projected to overtake hydropower in 2030. Thus, by the end of the decade, the generation matrix is expected to be 13.1% from hydropower, 13.4% from wind, 16.1% from PV, and 3% from other renewables.

In the context of Brazil, the primary source of generation, accounting for 60% of the total energy generated, is hydropower, equivalent to 425,996 GWh in 2023. However, similar to the global scenario, in recent decades, RES such as wind and PV generation have shown significant growth in the Brazilian energy generation matrix. Figure 2 illustrates the evolution of electricity generation sources in the country from 2000 to 2023. Since 2010, solar and wind power generation have exhibited near-quadratic growth, reaching 50,632 GWh and 95,800 GWh, respectively, in 2023. These figures correspond to 7.2% and 13.5% of total global electricity generation (Empresa de Pesquisa Energética - EPE, 2024; IEA, 2025).

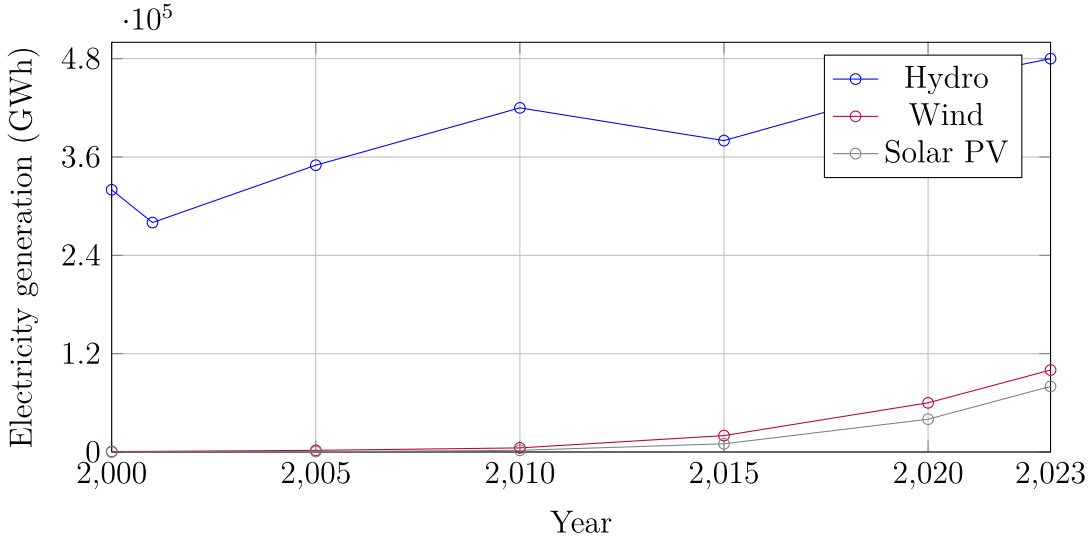
Notwithstanding these achievements, inefficiencies in energy forecasting result in some renewable energy being wasted (KOMARNICKI *et al.*, 2017). To mitigate this

Figure 1 – Share of renewable electricity generation by technology from 2000 to 2030.



Source: Adapted from IEA (2025).

Figure 2 – Electricity generation by source (non-combustible) in Brazil from 2000 to 2023.



Source: Adapted from IEA (2025).

waste, Energy Storage Systems (ESS), which have been employed since the early days of electrical systems, have become increasingly important, allowing for the storage of excess energy and offering additional services to the system. Nowadays, they play a crucial role in system stabilization and the development of local grids based on renewable energy sources. For this purpose, Battery Energy Storage Systems (BESS) are the most widely used in electrical grid applications (GYUK *et al.*, 2005; DIVYA; ØSTERGAARD, 2009). Due to advantages such as flexibility in site selection, shorter installation construction

times, and rapid response to system events, BESS are gaining increasing importance in the electric power market due to their various applications in generation, transmission, and distribution systems. In recent years, there has been a global increase in BESS installations, totaling more than 42 GW by the end of 2023 (IEA, 2024).

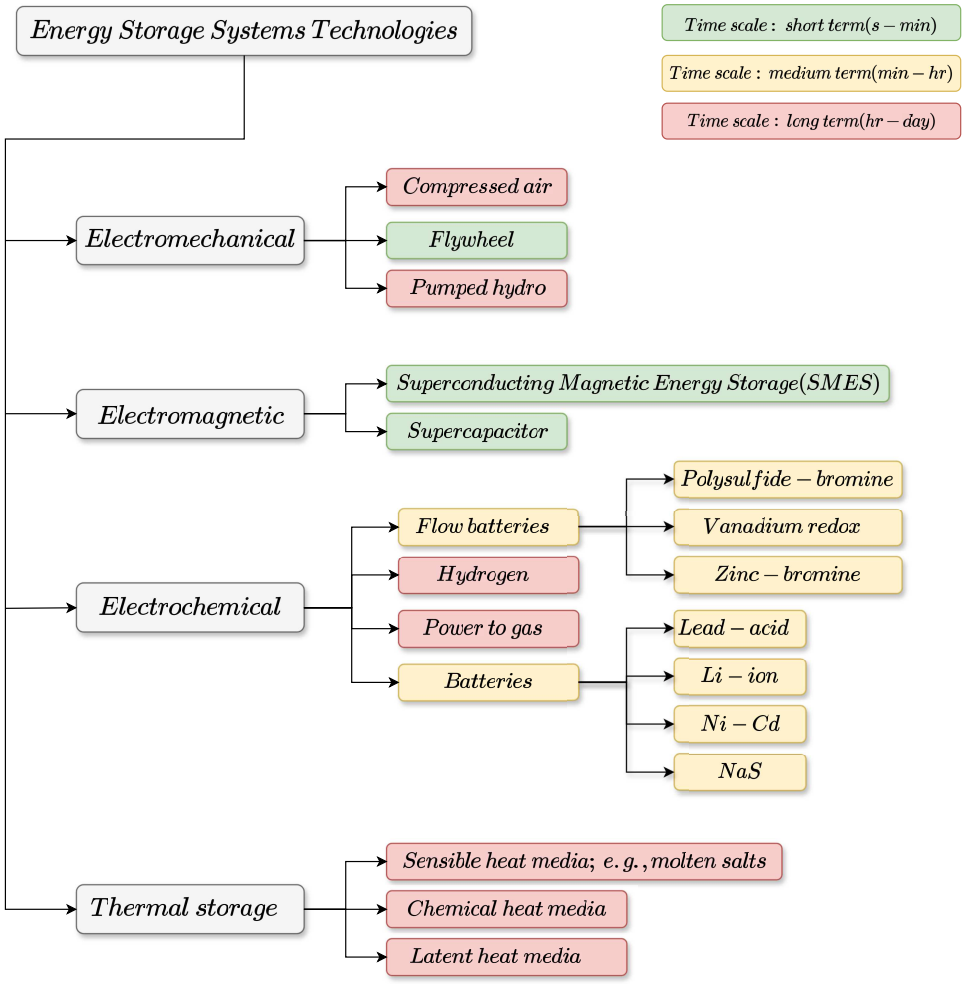
Since batteries provide energy in direct current (dc), power converters are commonly used to link the batteries to the alternating current (ac) electrical grid. There are several dc/ac converter topologies that can be used for BESS. In low-voltage storage applications, two-level converters are the most commonly used topologies. The efficiency and simplicity of their control system increase their popularity (TRINTIS; MUNK-NIELSEN; TEODORESCU, 2010). However, as the dc bus voltage and grid voltage increase, this topology becomes less advantageous, as it requires power semiconductors connected in series. An alternative that helps overcome the limitations of the previously mentioned converters is multilevel topologies, such as the Modular Multilevel Converter (MMC) patented by Marquardt (2001), owing to its promising advantages, such as modularity, simplified scalability, and reduced voltage and current stress on power switches, the MMC holds a prominent position over conventional two-level converters and other multilevel converter topologies (RAJU *et al.*, 2019). Additionally, the MMC has proven to be a highly versatile topology, with applications such as the Static Synchronous Compensator (STATCOM) (TIANQI *et al.*, 2019), a configuration that, when implemented alongside a BESS, is designated as an Energy Storage Static Synchronous Compensator (ES-STATCOM), which will be investigated in this work.

1.1.1 **Brief overview of Energy Storage Systems**

As outlined in the previous section, despite significant advancements in electricity generation from renewable sources, a considerable amount of energy continues to be wasted. Thus, ESS have emerged as a crucial technology for storing this otherwise unused energy, in light of this, these systems play important roles within the power system, namely time shifting and the provision of ancillary services. Time Shifting involves storing energy during periods of low demand and cost, and supplying it when demand and prices peak. This approach not only optimizes energy usage but also enables economic benefits through price differentials (SHAMIM *et al.*, 2019). In parallel, ESS are fundamental in delivering Ancillary Services that support the stability and reliability of the power grid. These services include frequency regulation, voltage stabilization, spinning reserves, electric supply capacity, black start and renewable capacity firming (REBOURS *et al.*, 2007; GLOBAL MARKET INSIGHTS, 2025). With the growing integration of nonlinear loads into the grid, power quality issues, such as flicker, voltage dips, and supply disruptions, have become increasingly common (DENHOLM *et al.*, 2010). ESS help address these challenges by providing rapid, responsive energy support, thereby improving overall grid performance and resilience.

The energy can be stored in ESS according to the load duration time, as shown in Figure 3. There are systems whose needs require a time scale of long, medium, and short durations, respectively, ranging from hours to days, minutes to hours, and seconds to minutes. Hence, the energy storage technology choice depends on the power and energy ratings, response time, operating cycles, weight, volume, temperature and also the choice is defined according to the service provided and the time of use (ARGYROU; CHRISTODOULIDES; KALOGIROU, 2018).

Figure 3 – Energy storage systems technologies.

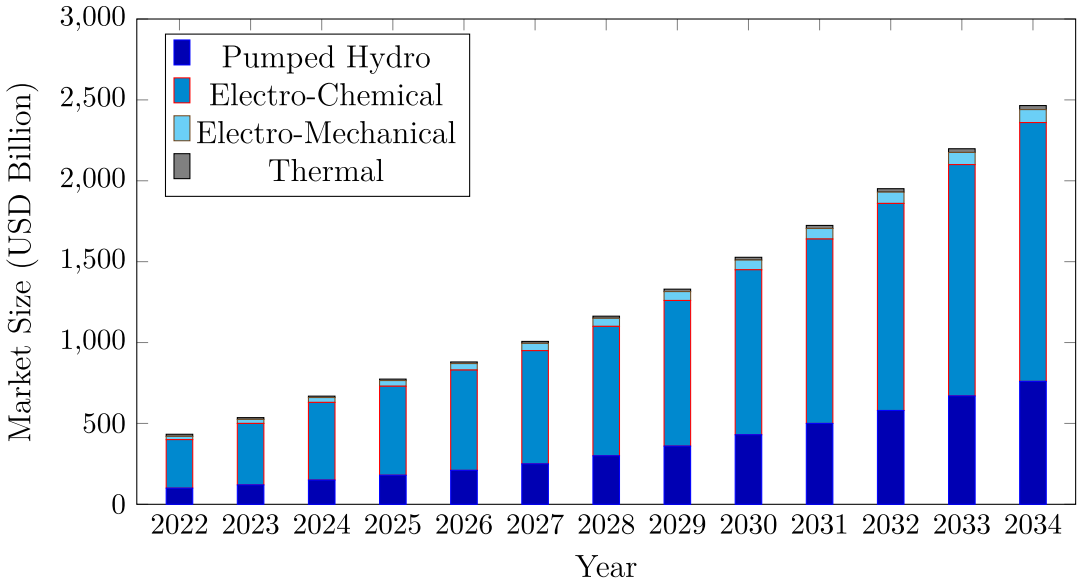


Source: Adapted from Rufer (2017).

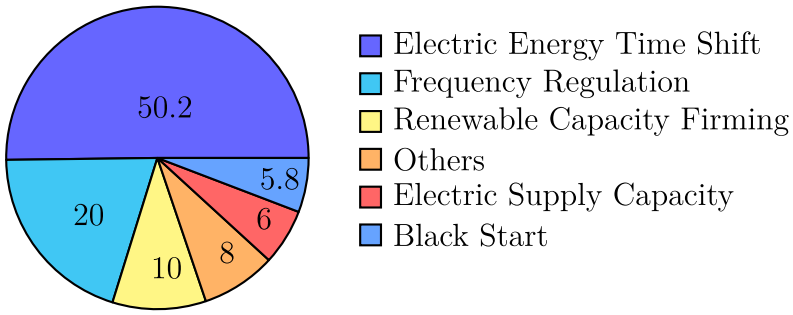
The growing importance of ESS is also demonstrated by the substantial size of their global market. Figure 4(a) presents the projected global market size by energy storage technology from 2024 to 2034, in which the ESS reached USD 433 billion, USD 535.8 billion and USD 668.7 billion in 2022, 2023 and 2024, respectively, and is expected to reach USD 5.12 trillion by 2034. It is noteworthy that electrochemical energy storage technologies show a sharp growth trend in the coming years. Nowadays, the ESS market by application is categorized into electric energy time shift, electric supply capacity, black start, renewable capacity firming, frequency regulation, and others. Among these, the

electric energy time shift segment held the largest share, accounting for over 50.2% of the market revenue in 2024 as illustrated in Figure 4(b), however, the remaining 49.8% pertains to ancillary services, which are also of critical importance.

Figure 4 – Energy storage systems global market.



(a)



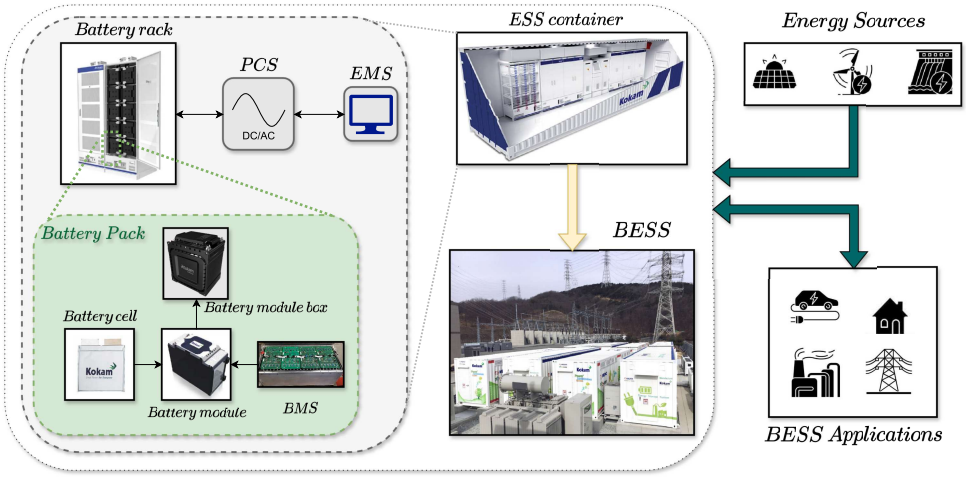
(b)

Caption: (a) ESS market size by technology(USD Billion); (b) Percentage of ESS market reveneu by application.

Source: Adapted from GLOBAL MARKET INSIGHTS (2025) .

In the present work, the electrochemical ESS technology will be adopted, specifically batteries, whose characteristic comparisons will be discussed in the next chapter. For this application, the storage system that uses batteries or merely BESS, is presented in the schematic diagram shown in Figure 5, and it consists of three main components: the Energy Management System (EMS), the battery rack, and the Power Conversion System (PCS). The EMS is responsible for overseeing battery operation by monitoring key electrical and thermal parameters through sensors, and managing overall functionality via a supervisory control system. At the core of the storage unit is the battery cell, which serves as the basic energy storage element. Cells are connected in series and/or parallel to

Figure 5 – Schematic of a Battery Energy Storage Systems.



Source: Prepared by the author (2025).

form modules, which are monitored by the Battery Management System (BMS). The BMS tracks vital information such as charge level, current, voltage, and temperature, ensuring safe and efficient operation. These components are housed within a battery module box to provide system protection, and multiple modules are assembled into a rack to scale the storage capacity. The PCS, a crucial interface between the battery system and the electrical grid, manages the bidirectional flow of power. It is typically installed in larger enclosures, such as containers, to accommodate system requirements and facilitate grid integration.

The global market for BESS features a diverse array of technologies that vary in battery chemistry, scale, application, and design. Several manufacturers lead this sector with innovative and widely adopted solutions across residential, commercial, and utility-scale applications. Table 1 outlines some of the main players in the global BESS industry, including their country of origin and primary areas of focus. Many companies operating in the power systems sector have begun to specialize in and commercialize BESS technologies. Industry leaders such as ABB, Samsung, and Siemens offer a range of solutions, including standalone BESS units and integrated configurations such as ES-STATCOM. Thus, Table 2 provides an overview of some examples from BESS projects installed worldwide between 2015 and 2022.

A critical feature of a BESS is that each battery rack operates independently, resulting in varying charge and discharge levels during operation. This imbalance can lead to some racks becoming overcharged while others are overdischarged, which negatively impacts battery lifespan (REIHANI *et al.*, 2016), degrades system performance, and may even cause system failure. To address this issue, equalization control must be implemented across the battery racks within a BESS (GALLARDO-LOZANO *et al.*, 2014). Research on battery equalization methods generally focuses on three key areas: strategies for balancing

Table 1 – Main BESS manufacturers.

Company	**Country**	**Short Description**
NextEra Energy	USA	Renewable energy + large-scale operational storage.
ABB	Switzerland/Sweden	Modular BESS for solar, transport, utilities, industry.
BYD	China	Utility-scale, commercial, and small battery storage.
Panasonic	Japan	EverVolt residential storage (11–120 kWh).
Toshiba	Japan	Super Charge ion Battery (SCiB) systems for public and industrial use.
Fluence	Germany/USA	Grid, solar, and commercial BESS (Gridstack, Sunstack, Edgestack).
Samsung SDI	South Korea	BESS for residential to utility-scale (kWh to MWh).
LG Chem	South Korea	Residential lithium-ion solar storage (RESU).
General Electric	USA	Standalone and hybrid BESS (solar, wind, thermal).
Hitachi	Japan	Modular BESS for commercial/industrial, hybrid-ready.
Tesla	USA	Powerwall (residential) and Powerpack (commercial/industrial).
NEC Corporation	Japan	Containerized BESS (20–53 ft) with AEROS® software.
Johnson Controls	USA	Containerized lithium-ion BESS (50–5000 kWh).
Kokam	South Korea	Developer of lithium polymer based energy storage solutions.
Siemens	Germany	Developer of modular BESS for utilities, industry and ancillary services.

Source: Adapted from INTEGRA SOURCES (2024).

the state of charge (SoC), defining SoC balancing limits, and balancing the state of health (SoH). In this work, however, the focus is placed specifically on a SoC balancing strategy for battery racks within a BESS, employing a STATCOM as the PCS.

1.1.2 **Brief overview of ES-STATCOM**

The implementation of ES-STATCOM systems in medium voltage grids depends on the services provided and agreements with local power system operators (CUPERTINO *et al.*, 2020). When combined with battery energy storage, ES-STATCOM can provide a diverse set of grid services, each offering unique advantages. Table 3 summarizes some of these services.

Table 2 – Examples of BESS project by applications.

Project Name	**Location**	**Power/Energy**	**Application**
Stafford Hill	Vermont, USA	4MW/3.4MWh	Peak shaving.
Hornsdale Power Reserve	South Australia	100MW/129MWh	Ancillary support.
Mt Newman	Western Australia	30MW/11.4MWh	Voltage regulation
Marengo	Illinois, USA	20MW/10MWh	Frequency regulation
AES Kilroot	Ireland	10MW/5MWh	Frequency response

Source: Adapted from SAFT (2024).

Table 3 – Services provided by ES-STATCOM.

Provided Service	**Description**
Backup power	Stores energy during generation and supplies it when sources like PV are unavailable.
Black start capability	Helps restart the power system after a blackout, minimizing outage time.
Frequency support	Maintains frequency stability in islanded microgrids, ensuring continuous supply.
Load leveling (arbitrage)	Charges when energy prices are low and discharges when prices are high to optimize costs.
Peak shaving	Reduces peak demand charges by storing energy in low-demand periods and using it during peaks.
Power quality improvement	Improves voltage and compensates harmonics, enhancing network power quality.
Power smoothing for renewable generation	Mitigates output fluctuations from renewables like wind and solar.
Spinning reserve	Provides fast backup during sudden load changes, reducing reliance on traditional reserves.
Transmission and Distribution (T&D) upgrade deferral	Eases network stress at critical points, postponing costly infrastructure upgrades.
Voltage support	Supplies reactive power to help recover voltage during faults and disturbances.

Source: Adapted from AMORIM (2019).

The performance and versatility of ES-STATCOM systems are significantly influenced by the used converter's topologies. When integrated into the power grid, these systems typically consist of a battery pack, a dc/dc stage, and a dc/ac stage, each con-

tributing to the control and transformation of electrical energy. The choice of topology affects critical operational aspects such as efficiency, power quality, and fault response.

Among the conventional options, the two-level converter remains one of the most commonly implemented due to its structural simplicity. Within this category, configurations such as the Voltage Source Converter (VSC), Z-source converter (ZSI), and Quasi-Z-source converter (qZSI) are frequently adopted in ES-STATCOM designs. These alternatives address several of the limitations found in standard VSC systems, particularly in terms of voltage boosting and current ripple control (VAZQUEZ *et al.*, 2010; KRISHNAMOORTHY *et al.*, 2013; KEBEDE *et al.*, 2022). To ensure smooth integration with the grid and reduce harmonic distortion, low-pass filters like LC and LCL are often employed.

The three-level converter topology offers an attractive option for applications demanding higher output voltage quality and improved harmonic performance. Within this class, the Neutral Point Clamped (NPC) converter and the flying capacitor converter are particularly relevant. The NPC architecture enhances the voltage output range and minimizes the need for extensive filtering; however, it also introduces greater complexity in modulation and control schemes (POU *et al.*, 2005; ARIFUJJAMAN, 2015).

The flying capacitor topology, also within the three-level category, uses capacitors in place of clamping diodes. This design enables dc voltage balancing directly through modulation techniques, offering a simpler and more adaptable solution for high-performance applications. Its efficient voltage management makes it well-suited for dynamic grid support operations in ES-STATCOM systems.

Cascaded multilevel converters have gained prominence due to their scalability and their ability to mitigate issues such as SoC imbalances across battery modules. These topologies utilize low-voltage switching devices and operate at lower switching frequencies, which improves system efficiency and extends component lifespan. Their enhanced voltage waveform quality and fault tolerance further bolster their appeal in grid connected energy storage systems (SOONG; LEHN, 2014a; FARIVAR *et al.*, 2022).

Different configurations of cascaded multilevel converters provide unique advantages. Star-connected systems are often more cost-effective in terms of hardware and implementation, while delta-connected versions typically exhibit superior dynamic performance, especially when responding to grid disturbances, whether symmetrical or asymmetrical (SOCHOR; AKAGI, 2015; BOSCAINO *et al.*, 2024). These attributes make cascaded topologies particularly suitable for flexible, fault resilient applications.

A notable variant in this context is the MMC, frequently implemented using configurations like the Double-Star (DS) topology (AKAGI, 2017). These converters allow for either centralized or decentralized battery arrangements – a topic that will be explored in more detail in the following chapter – depending on system design and application goals (MARQUARDT, 2001; SOONG; LEHN, 2014b; VASILADIOTIS; CHERIX; RUFER, 2015;

BASHIR *et al.*, 2023). The adaptability and modularity of the MMC have positioned it as a compelling choice for advanced ES-STATCOM deployments.

As previously highlighted, the advantages of the MMC make it a suitable choice for ES-STATCOM applications. Therefore, this topology will be used for the online balancing of the SoC of each submodule (SM) in the converter, and subsequently for the provision of ancillary services such as frequency support and voltage support to the grid, assessing the performance of the ES-STATCOM during these three operational cases.

1.2 OBJECTIVES

Given the increasing integration of RES and the associated challenges, such as intermittency and grid instability, the use of BESS has become essential. To address these operational challenges, this research proposes as its main objective the development and verification of an online SoC balancing strategy for BESS integrated with an ES-STATCOM based on a MMC.

To achieve this, the following specific objectives are pursued:

a) Investigate ESS technologies, ES-STATCOM concepts, SoC balancing methods and MMC advantages for grid support applications;

b) Model and design the MMC-based ES-STATCOM with a single stage distributed BESS configuration;

c) Propose and implement a control strategy for the ES-STATCOM output currents regulation;

d) Propose and implement the Circulating Current Suppressing Control (CCSC) to compensate the internal currents of the ES-STATCOM;

e) Propose and implement an online SoC balancing algorithm;

f) Simulate and compare results of the SoC balancing process approaches with active and reactive power;

g) Simulate and evaluate the ES-STATCOM dynamics during the ancillary services simulation cases.

1.3 CONTRIBUTIONS

As discussed previously, this work presents the following main contributions:

a) Comprehensive modeling of an MMC-based ES-STATCOM with single stage distributed BESS configuration;

b) Proposal and verification of an online SoC balancing strategy in different approaches using active and reactive power for ES-STATCOM applications;

c) Design and verification of a simple and effective control framework for an ES-STATCOM current regulation and circulating current suppression;

d) Assessment of the proposed ES-STATCOM effectiveness in providing ancillary services.

1.4 MASTER THESIS OUTLINE

After the Chapter 1, the master thesis is structured into four core chapters and two appendices, as follow:

Chapter 2 introduces the ES-STATCOM, detailing its structure, battery technologies, modulation techniques, and SoC balancing methods that support the proposed system design.

Chapter 3 presents the system modeling and control design, covering mathematical formulations, control strategies for current regulation, circulating current suppression, and the implementation of the online SoC balancing algorithm.

Chapter 4 discusses simulation results for SoC balancing under different strategies using instantaneous power, highlighting the system's dynamic performance and validating the effectiveness of the proposed algorithm.

Chapter 5 evaluates the system's capacity to provide ancillary services, focusing on frequency and voltage support, through simulations under various grid conditions and disturbances.

Chapter 6 synthesizes the main conclusions, emphasizing the effectiveness of the proposed control framework, outline future research directions for further enhancing BESS integration.

Finally, Appendix A and Appendix B provide supplementary mathematical formulations essential for the control and synchronization methods employed, referring respectively, to Park's Transformation and Double Second Order Generalized Integrator - Phase Locked Loop.

1.5 LIST OF PUBLICATIONS

1.5.1 Published Conference Papers

[1] Peralta, J. A., Sanseverino, J. P., de Almeida, P. M., & Barbosa, P. G. "Controle Independente dos Braços Superiores e Inferiores de um Conversor Multinível Modular com Base na Teoria das Potências Instantâneas". XI Simpósio Brasileiro de Sistemas Elétricos (SBSE 2025), São João del Rei, Minas Gerais, Brasil, 2025.

[2] Garay, J. A. P., Franklin, L. R., de Almeida, P. M., & Barbosa, P. G. “Compensação de Correntes Circulantes em Conversores Multiníveis Modulares por Meio da Energia Armazenada nos Submódulos”. XXV Congresso Brasileiro de Automática, Barra da Tijuca, Rio de Janeiro, Brasil, 2024.

[3] Franklin, L. R., da Silva, J. L., Júnior, D. C., Peralta, J. A., de Almeida, P. M., & Barbosa, P. G. (2023, November). “Comparative Performance of Direct and Energy-based Controllers to Compensate Internal Currents of Modular Multilevel Converters”. In 2023 IEEE 8th Southern Power Electronics Conference and 17th Brazilian Power Electronics Conference (SPEC/COBEP) (pp. 1-8).

[4] Peralta, J. A., de Almeida, P. M., & Barbosa, P. G. “Online SoC Balancing Strategy for MMC-Based Battery Energy Storage Systems”. 18th Brazilian Power Electronics Conference (COBEP 2025), Vitória/ES, Brazil, 2025.

[5] Sanseverino, J. P., Peralta, J. A., Almeida, A. O., de Almeida, P. M., & Barbosa, P. G. “Strategy to Compensate Internal Currents of Modular Multilevel Converters Based on Independent Control of the Upper and Lower Arms”. 18th Brazilian Power Electronics Conference (COBEP 2025), Vitória/ES, Brazil, 2025.

2 ENERGY STORAGE STATIC SYNCHRONOUS COMPENSATOR

There are several power electronics converter topologies suitable for use as ES-STATCOM. As discussed in the introduction chapter, this work adopts the implementation of the MMC for the ES-STATCOM applications. However, specific variations within the selected topology, as depicted in Figure 6, must still be defined.

The MMC shown in Figure 6(a) and Figure 6(b) is represented as a generic leg, as described by Wang *et al.* (2020). The total number of legs in such a converter corresponds to the number of phases in the connected ac system, in which $k \in \{ a, b, c\}$. In an ES-STATCOM, the battery arrangement can be connected directly to the dc bus, as shown in Figure 6(a); this configuration is referred to as centralized. An alternative approach involves connecting individual battery racks to each SM of the converter, as shown in Figure 6(b); this arrangement is known as the distributed configuration.

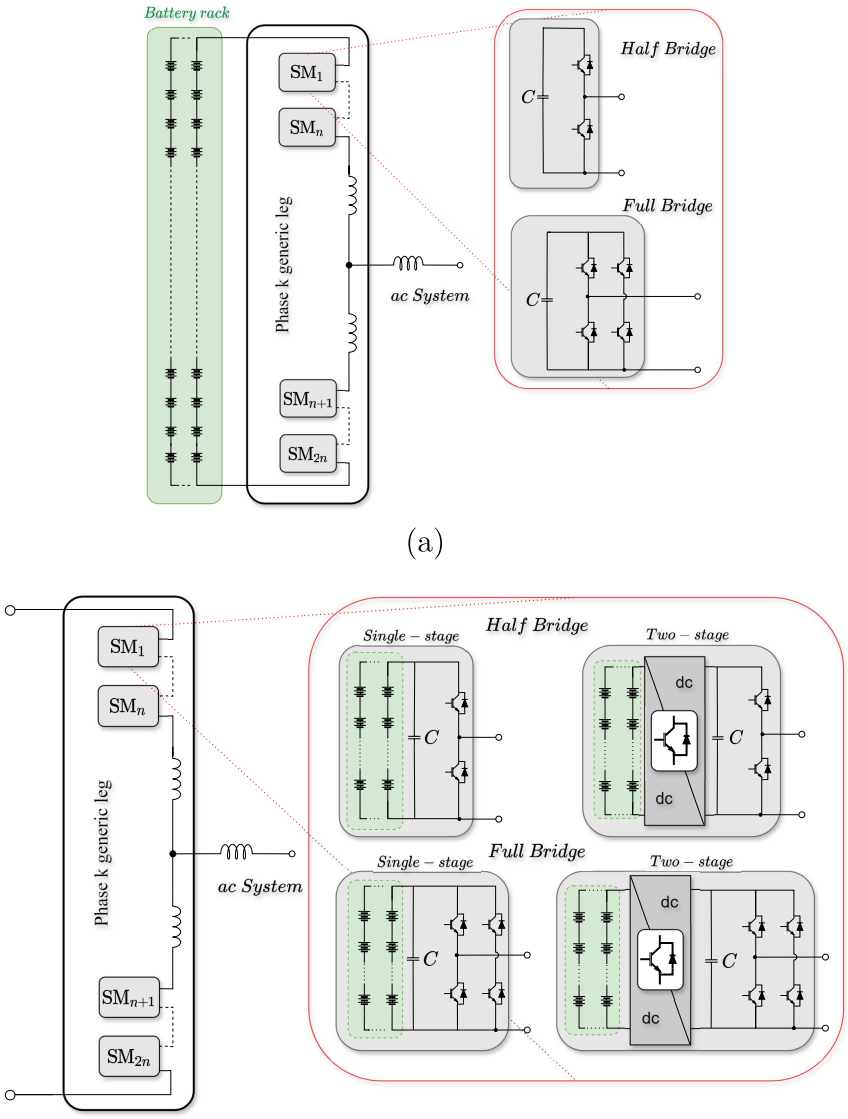
The centralized arrangement becomes less advantageous when compared to the distributed system, as it necessitates the use of long battery strings to achieve the required dc bus voltage levels. To leverage the inherent modularity of the converter, batteries can instead be connected directly to each SM. In this distributed arrangement, the battery racks may either be integrated directly into the SM in a single-stage configuration or interfaced through a dc/dc converter in a two-stage configuration, as illustrated in Figure 6(b) (WANG *et al.*, 2016). The distributed architecture offers several benefits, including higher efficiency, improved reliability, and more flexible control strategies. As a three-terminal system, it facilitates effective interconnection and decoupling control between ac and dc systems, thereby serving as a robust energy storage solution capable of delivering power smoothing and buffering functionalities (TRINTIS; MUNK-NIELSEN; TEODORESCU, 2011; KAWAKAMI *et al.*, 2014; MA *et al.*, 2023).

Different converter configurations can be used in the SM (DU *et al.*, 2018). In general, the most common ones are the DS Half-bridge Submodule (HBSM) and Full-bridge Submodule (FBSM) shown in Figure 6. Some comparisons between these two SM configurations applied in MMC are discussed in Chen, Li e Cai (2016). However, since a complex topology is not required for the purposes of this work, aiming for simplicity and lower cost, the HBSM has been adopted. Thus, the ES-STATCOM to be addressed here will have a distributed single-stage configuration.

2.1 BASIC CHARACTERISTICS OF ES-STATCOM

Figure 7 illustrates a three-phase ES-STATCOM connected to the ac system, implemented using a distributed single-stage configuration in a DS MMC. As previously described using the generic leg representation, the converter consists of a number of legs equal to the number of phases in the grid. Each leg is subdivided into two arms: an upper

Figure 6 – Basic ES-STATCOM configurations.

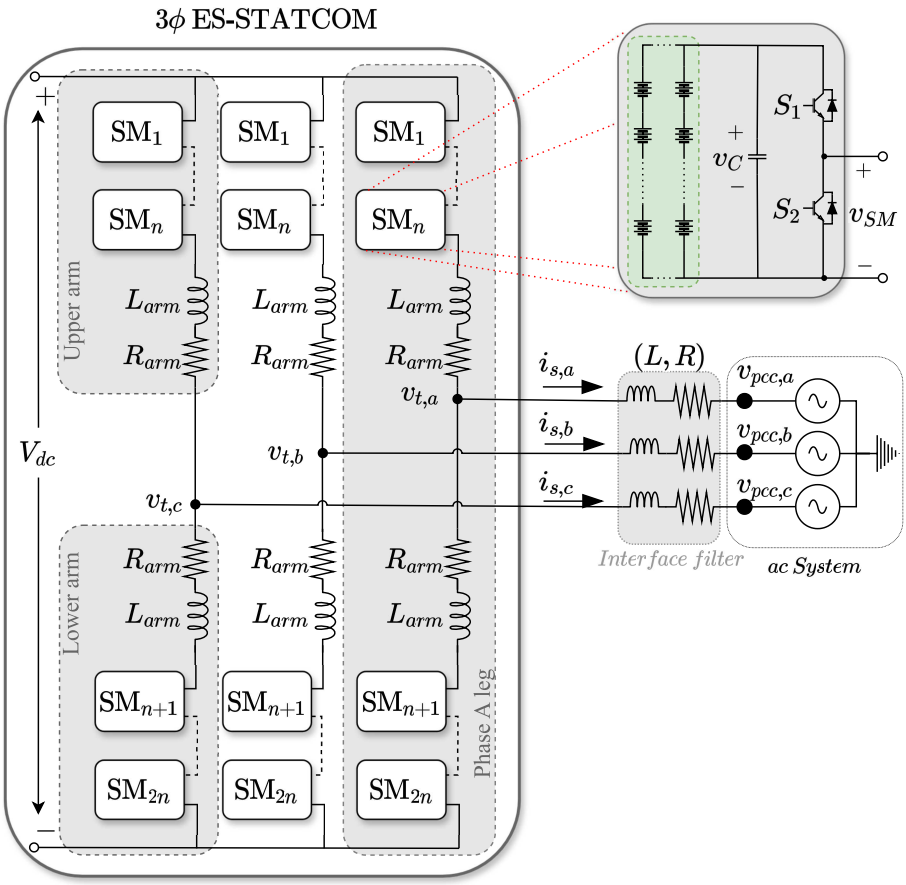


Caption: (a) DS Half-Bridge or DS Full-Bridge with BESS centralized; (b) DS Half-Bridge or DS Full-Bridge with BESS distributed in single-stage or two-stage configuration.

Source: Prepared by the author (2025).

arm (positive pole) and a lower arm (negative pole). Each arm comprises N submodules connected in series, along with an arm inductor L_{arm}. The total arm resistance R_{arm} accounts for the conduction resistance of the semiconductor switches within the SM as well as the arm inductance L_{arm}. The converter's output terminal is connected in series with an impedance $Z = (R + sL)$, acting as a first-order filter to mitigate harmonics, and subsequently connected to the Point of Common Coupling (PCC) with the grid. While its input terminals remain open-circuited, given that energy exchange is managed internally via the battery-integrated SM.

Figure 7 – Single-stage DS HBSM distributed 3ϕ ES-STATCOM.



Source: Prepared by the author (2025).

2.1.1 Battery technologies used in ESS

The process of storing and releasing energy in batteries is based on reversible oxidation-reduction (redox) electrochemical reactions, which convert electrical energy into chemical energy during charging and reverse the process during discharging (RUFER, 2017). The selection of a battery involves evaluating several factors, including energy density, efficiency, service life, self-discharge characteristics, recyclability of materials, and cost.

A battery consists of multiple electrochemical cells arranged in series and/or parallel and it is classified as either primary or secondary depending on its rechargeability, in which each cell contains a cathode and an anode, immersed in an electrolyte that may be solid, liquid, or viscous in form (IBRAHIM; ILINCA; PERRON, 2008; DÍAZ-GONZÁLEZ *et al.*, 2013). Primary batteries are intended for single use and are typically found in low-power devices like watches and calculators. In contrast, secondary batteries are rechargeable and commonly used in smartphones, laptops, electric vehicles, and Uninterruptible Power Supply (UPS) systems (TAVARES; GALDINO, 2014).

Table 4 presents various types of batteries used in ESS, along with brief descriptions

to facilitate a comparison of the technologies. Despite on sodium-sulphur (NaS) and flow batteries could be used in BESS applications, Li-ion batteries are lighter, more compact, and more powerful than other types, making them especially attractive for consumer electronics devices (MAHLIA *et al.*, 2014). Therefore this battery technology was selected for this study due to its notable advantages.

Table 4 – Comparison of different battery types.

Type	**Description**
Lead-Acid Batteries	Oldest secondary cell technology, widely used for low-cost, short-response applications. Short lifespan and low energy density.
Lead Carbon Batteries (PbC)	Improved Pb-acid technology with better performance, longer life, and lower sulfation. Used in grid and renewable integration.
Nickel-Cadmium (NiCd) Batteries	Rechargeable batteries known for reliability and performance at low temperatures, but prone to memory effect and environmental concerns.
Nickel-Metal Hydride (NiMH) Batteries	More energy-efficient than NiCd, used in power tools, hybrid vehicles, and electronics with higher capacity and lifespan.
Nickel-Iron (NiFe) Batteries	Known for robustness, high-cycle life, but lower energy density. Used in industrial applications.
Sodium-Sulphur (NaS) Batteries	High-energy, high-efficiency batteries, used in large-scale applications like grid energy storage. Requires high operating temperature.
Flow Batteries	Rechargeable batteries with electrolytes stored in external tanks, offering high safety, long lifespan, and flexibility in power applications.
Lithium-Ion (Li-ion) Batteries	Popular in portable electronics and electric vehicles, offering high energy density, but sensitive to temperature and depth of discharge.

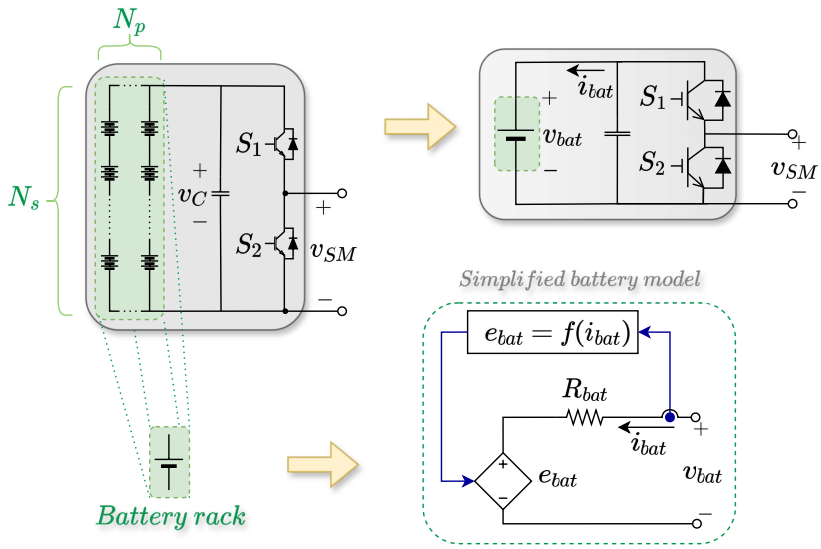
Source: Adapted from Pinto *et al.* (2022).

2.1.2 **Submodule characteristics**

The battery rack model connected in each HBSM is depicted in Figure 8 and represents a simplified equivalent of a battery rack composed of N_s battery packs in series-connected, in N_p parallel strings, which are composed of hundreds of Kokam lithium-ion cells, model SLPB120216216 (Kokam, 2019). The number of packs in each battery rack forming a submodule is determined based on the required voltage per SM and the maximum allowable voltage per pack, while the total number of submodules is defined according to the specified dc bus voltage, ensuring the system meets the required energy storage

capacity, this will be further addressed in the following chapter. The no-load voltage e_{bat} is expressed as a function of the battery current i_{bat}, capturing the model's behavior by incorporating the SoC under different discharge rates and temperature variations; further details will be presented in the next chapter.

Figure 8 – Battery rack model connected to the HBSM.



Source: Prepared by the author (2025).

Each SM is composed with a pair of Insulated Gate Bipolar Transistor (IGBT) that are controlled in a coordinated manner, enabling two main distinct operating states: inserted or bypassed, as summarized in Table 5. When the SM is inserted into the ES-STATCOM leg configuration, the upper IGBT is closed, and the lower IGBT remains opened. In this state, the voltage at the submodule output terminals is equal to the voltage of the associated battery rack, which also corresponds to the voltage across the dc capacitor. In contrast, when bypassed, there are three possible combinations of the IGBT switch positions: the upper IGBT is opened and the lower IGBT is closed, both are opened, or both are closed, with the latter combination assuming a blocked state; in all of these cases, the SM output voltage is zero.

In the first possible condition for the forbidden state in Table 5, both upper and lower IGBT are opened, this case is forbidden if its refers to a structural opening of the switches, because the SM are connected in series within the arm, and in this situation, the SM would be opening the arm circuit and it will appear a high impedance. The last forbidden state condition occurs when both switches of the SM are closed, then both IGBT conduct, creating a short-circuit across the dc bus, which is a critical fault. Thus the SM is defined in a forbidden state, which can be solved by using a dead time between the switching of the two IGBT. Finally, the dead time state, avoiding both switches being simultaneously closed, it will be only allowed if its occurs in a μs scale of time. The voltage at the terminals of the SM will depend on which switch was conducting immediately before

the dead time is applied, as shown in the Table 5. Since the scope of this work is focused primarily on the balancing of the SoC and the overall operation of the ES-STATCOM, only the first two operating states of the SM presented earlier will be considered in the study.

Table 5 – Operating modes of the HBSM.

Status	S_1	S_2	v_{SM}
Inserted	1	0	v_{bat}
Bypassed	0	1	0
Blocked	0	0	0 or v_{bat} ‡
Short-circuit	1	1	Forbidden

‡ depending on the polarity of the current.

Source: Prepared by the author (2025).

Figure 9 aims to provide a better understanding of the operating modes of the HBSM, under battery rack charging and discharging conditions. In Figure 9(a), the SM is inserted, with the upper IGBT closed and the lower IGBT opened, and the current in the j arm of the k leg of the ES-STATCOM flows into the SM, charging the battery rack in parallel with the dc capacitor, causing the output voltage to be v_{bat}. Figure 9(b) illustrates the condition from Table 5 when the SM is bypassed. In this situation, the upper IGBT is opened and the lower IGBT is closed, preventing current from entering the SM. Figures 9(c) and 9(d) show the arm current paths during the battery rack discharging conditions in line with the discussed above.

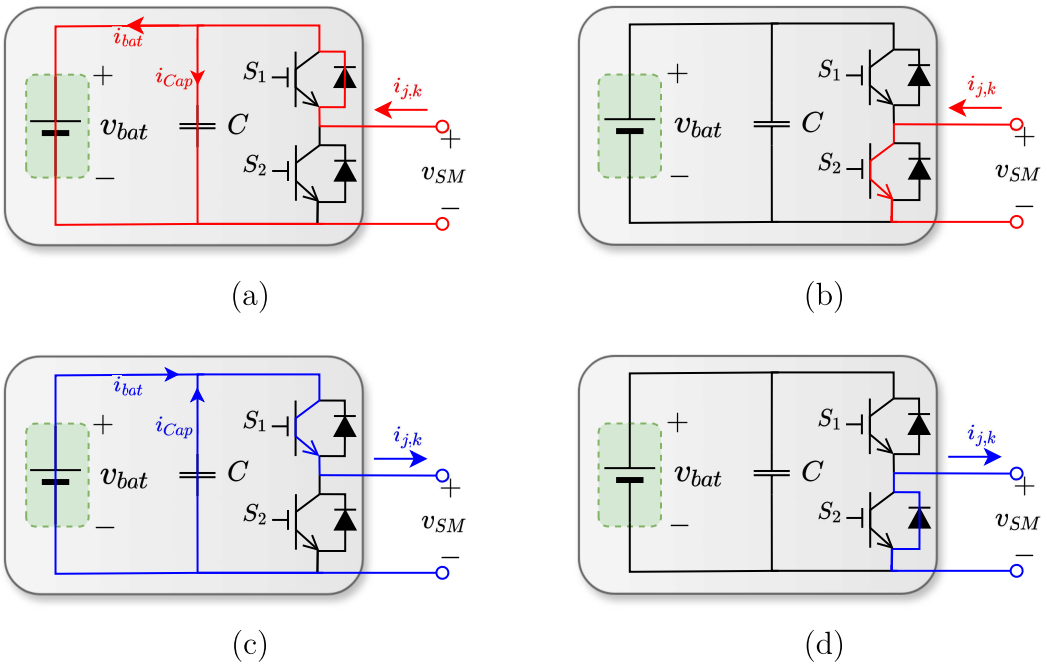
2.1.3 **Modulation techniques**

There are several multi-carrier Pulse Width Modulation (PWM) techniques that can be used for controlling the semiconductor switches in the ES-STATCOM converter (OMER; KUMAR; SURJAN, 2014). These strategies are grouped into Phase-shifted PWM Carrier (PS-PWM) and Level-shifted PWM Carrier (LS-PWM).

In PS-PWM, each carrier signal has identical amplitude and frequency but is phase-displaced by an angle of ($2\pi/N$ rad) relative to one another, where N represents the number of SM per arm of the MMC. This phase displacement effectively increases the equivalent carrier frequency seen at the output, resulting in improved harmonic performance without increasing individual switching frequencies.

On the other hand, in LS-PWM, the carriers are vertically stacked within the same amplitude range, effectively subdividing the modulation window into N bands. LS-PWM methods are further classified into three variants: Phase Disposition PWM Carrier (PD-PWM), where all carriers are in phase; Phase Opposition Disposition PWM Carrier (POD-PWM), where carriers above and below the zero reference are phase-opposed;

Figure 9 – Current flow according to its direction and the operating states of the SM.



Caption: (a) Inserted SM with incoming current; (b) Bypassed SM with incoming current; (c) Inserted SM with outgoing current; (d) Bypassed SM with outgoing current.

Source: Prepared by the autor (2025).

and Alternate Phase Opposition Disposition PWM Carrier (APOD-PWM), where adjacent carriers are phase-opposed. Each method offers distinct advantages in terms of harmonic distribution and switching losses (RAMU; KUMAR; SRINIVAS, 2022).

Moreover, the synthesized output voltage waveform can exhibit either $(N + 1)$ or $(2N + 1)$ discrete levels. This depends on whether a single reference signal or two complementary reference signals are compared with the set of triangular carriers, respectively. In the present work, the PD-PWM strategy was employed to define the switching pattern of the ES-STATCOM, thereby enabling the generation of ac output voltages with $(2N + 1)$ distinct voltage levels.

2.1.4 SoC balancing methods overview

As discussed in the previous chapter, each SM of the ES-STATCOM exhibits distinct electrical characteristics, with variations in charging and discharging levels during operation. Such variations introduce challenges related to the maintenance of voltage and energy uniformity among submodules, which must be properly addressed to ensure the system's reliability and performance. Within this context, it was previously mentioned that battery equalization methods primarily focus on three critical aspects: the development of strategies for balancing the SoC, the definition of SoC balancing limits, and the

consideration of strategies to balance the SoH across the energy storage modules.

Focusing specifically on SoC balancing, a wide range of strategies has been proposed in the literature, each offering specific advantages depending on the system architecture and operational goals. These techniques can be broadly classified into five main groups: dissipative methods, capacitor-based methods, inductor-based methods, transformer-based methods, and converter-based methods. Below, the main techniques from each group are described, along with their operational characteristics, advantages, and drawbacks; considering Litium-ion battery packs, in which n_{cells} is the number of cells in the pack:

- **Fixed resistor method**: This dissipative method uses n_{cells} resistors to equalize cell voltages by dissipating excess energy as heat. Its primary advantages are simplicity and low cost, as noted by Wei *et al.* (2017). However, it suffers from low balancing speed and continuous energy loss through heat dissipation, which can result in unwanted pack discharge.

- **Switched resistor method**: By integrating n_{cells} resistors and n_{cells} switches, this method allows more control over the balancing process, enabling relatively higher balancing speed and lower loss compared to fixed resistors. Nevertheless, according to Zhang *et al.* (2016), it increases system cost and remains limited to low-power applications due to the need to dissipate energy.

- **Double-tiered switched capacitors**: In this capacitor-based technique, n_{cells} capacitors and $2n_{cells}$ switches are used to redistribute charge. As shown in Baughman e Ferdowsi (2008), it offers modularity, simple control, and adequate balancing speed. The downside lies in the high number of required switches and elevated cost.

- **Single switched capacitor**: This approach uses one capacitor, one resistor, and $n_{cells} + 5$ switches, offering a more component-efficient architecture. It provides improved efficiency, but, as also discussed in Baughman e Ferdowsi (2008), the balancing speed remains low.

- **Single inductor method**: This inductor-based method uses one inductor along with $2n_{cells}$ switches and $2n_{cells}$ diodes to transfer energy between cells via magnetic storage. As detailed by Vardhan *et al.* (2017), it achieves satisfactory balancing speed and higher efficiency. However, it introduces considerable control complexity and cost.

- **Multi-inductor method**: Incorporating $n_{cells} - 1$ inductors and $2n_{cells} - 2$ switches, this method simplifies control compared to other inductor-based solutions and provides good balancing speed. Cui *et al.* (2017a) highlight its main drawback as being the high implementation cost.

- **Multiple transformer method**: This transformer-based technique employs n_{cells} transformers, a switch, and n_{cells} diodes. It supports good modularity and balancing speed but is associated with very high cost, reduced efficiency, and larger physical dimensions (EINHORN; ROESSLER; FLEIG, 2011).

- **Multi-winding transformer method**: By using a single 1:n_{cells} transformer with a switch and n_{cells} diodes, this method achieves relatively compact implementation. Nonetheless, as shown in Einhorn, Roessler e Fleig (2011), it is less efficient and limited to a smaller number of cells.

- **Switched transformer method**: Utilizing a single transformer, $n_{cells} + 6$ switches, and one diode, this method provides lower magnetic losses and compactness. Imtiaz, Khan e Kamath (2011) note that it demands complex control logic and has high associated cost.

- **Buck-boost converter method**: This converter-based method uses n_{cells} converters to manage energy actively between cells. Qays *et al.* (2020) demonstrate that it offers good efficiency and satisfactory balancing speed, albeit with increased size, cost, and control complexity.

- **Cuk converter method**: Composed of $n_{cells} - 1$ converters, this technique achieves good balancing performance with satisfactory efficiency. Yan *et al.* (2010) indicate that complex control is required, and the system has relatively large size.

- **Flyback converter method**: Involving one converter and $2n_{cells}$ switches with a single transformer, this method achieves fast balancing with fewer components and simpler control. Cui *et al.* (2017b) emphasize that its main disadvantage is the requirement of a transformer.

- **Multi-module full-bridge converter**: This scalable method uses n_{cells} converters and is suitable for high-power systems. Chatzinikolaou e Rogers (2016) show that it delivers good balancing speed but comes at the cost of high complexity, large size, and expense.

- **Quasi-resonant converter**: Employing $n_{cells}-1$ converters, this method is relatively easy to implement and achieves high efficiency. According to Lee e Cheng (2006), it is hindered by high cost and significant physical size.

More recently, innovative approaches under the *smart battery* concept (TEODORESCU *et al.*, 2021) have been introduced, aiming to optimize not only SoC but also thermal management, SoH balancing, and real-time energy routing to improve overall system efficiency and extend the battery life-cycle.

The previously mentioned SoC balancing techniques can be implemented in a BESS either in an online or offline manner. These two approaches refer to how the balancing process is carried out: in the online method, balancing takes place while the BESS remains connected to the grid; whereas in the offline method, the BESS is disconnected from the grid during the balancing process, and energy is exchanged directly between the battery cells.

In light of the above, and considering that the objectives of this work aim to be achieved with simplicity and efficiency as a first step on the investigation, this study will investigate the online SoC balancing of the battery packs integrated into the ES-STATCOM architecture presented earlier in this chapter. For simplicity and computational efficiency, the balancing algorithm adopted is based on the bubble sort method (GHETTI *et al.*, 2017). Further details regarding the modulation and SoC balancing algorithm will be provided in the following chapter.

2.2 CHAPTER REMARKS

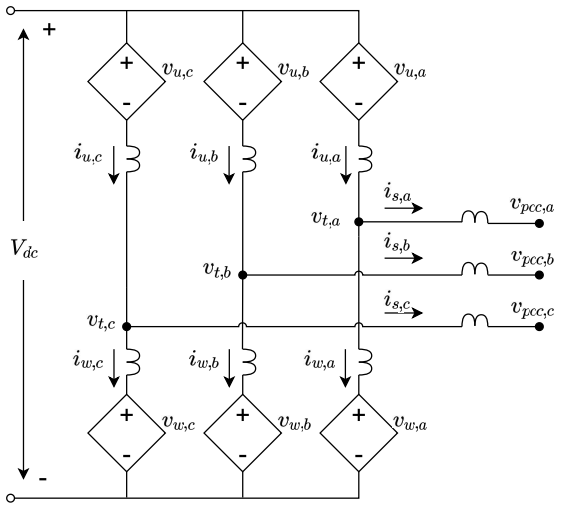
This chapter has outlined the fundamental operating principles of the ES-STATCOM system. A comprehensive discussion was provided regarding the different SM topologies and the possible configurations for integrating battery systems into the BESS converter. A brief overview of batteries technologies, such the structural and operational characteristics of the specific SM to be employed in this study were also described in detail, along with the type of lithium-ion battery technology selected for the ensuing analysis.

In addition, a concise yet technically grounded overview of the PWM techniques typically applied in such systems was presented, followed by a literature-based review of the main SoC balancing strategies. These discussions establish a necessary theoretical and bibliographical framework that underpins the subsequent development of the methodology and implementation strategies addressed in the next chapter.

3 MODELING, CONTROL AND DESIGN OF THE ES-STATCOM

In this chapter, the mathematical modeling describing the dynamics of the ES-STATCOM, illustrated and presented in Figure 7, will be developed, along with the control strategies to be employed for the output current regulation, the circulating currents through the MMC arms, the converter control mode, the SoC balancing algorithm, and the battery pack model, as well as the parameter settings of the converter.

Figure 10 – Equivalent circuit of the ES-STATCOM.



Source: Prepared by the author (2025).

Considering the direction of the currents indicated in the circuit of Figure 10, the following expressions can be established for each phase of the ES-STATCOM:

$$v_{t,k} - v_{pcc,k} = L_{eq}\frac{di_{s,k}}{dt} + R_{eq}i_{s,k} \ , \tag{3.1}$$

in which $v_{t,k}$ is the ES-STATCOM terminal voltage, $v_{pcc,k}$ is the voltage at the PCC, $i_{s,k}$ is the ES-STATCOM output current; and $L_{eq} = (L + \frac{L_{arm}}{2})$ and $R_{eq} = (R + \frac{R_{arm}}{2})$ represent the equivalent inductance and resistance seen from the ES-STATCOM terminals, respectively, with $k \in \{a,b,c\}$ denoting the phase index.

Neglecting the harmonics generated by the converter and assuming that the three-phase power grid of Figure 7 is balanced, the system given by (3.1) can be rewritten in the Synchronous Reference Frame (SRF) as follows:

$$\begin{aligned} v_{t,d} - v_{pcc,d} + \omega L_{eq} i_{s,q} &= L_{eq}\frac{di_{s,d}}{dt} + R_{eq}i_{s,d} \ , \\ v_{t,q} - v_{pcc,q} - \omega L_{eq} i_{s,d} &= L_{eq}\frac{di_{s,q}}{dt} + R_{eq}i_{s,q} \ , \end{aligned} \tag{3.2}$$

in which $v_{t,d}$, $v_{t,q}$, $v_{pcc,d}$, $v_{pcc,q}$, $i_{s,d}$ e $i_{s,q}$ are, respectively, the ES-STATCOM terminal voltages, PCC voltages , and the converter output currents in the synchronous dq reference frame, being $\omega = (d\theta/dt)$ the angular frequency of the voltages at the PCC.

The angle θ, used in the Park transformation (Appendix A) to derive (3.2), is extracted from the voltages at the PCC by a Double Second Order Generalized Integrator (DSOGI)-Phase-Locked Loop (PLL)(Appendix B). Additionally, the zero-sequence equation was neglected in the previous system, since the ES-STATCOM is three-wire only.

By applying the Laplace transform to (3.2) and rearranging the expressions to isolate the converter output currents, the following representation is obtained:

$$\begin{aligned} I_{s,d}(s) &= \frac{1}{sL_{eq} + R_{eq}} \left(V_{t,d}(s) - V_{pcc,d}(s) + \omega L_{eq} I_{s,q}(s) \right), \\ I_{s,q}(s) &= \frac{1}{sL_{eq} + R_{eq}} \left(V_{t,q}(s) - V_{pcc,q}(s) - \omega L_{eq} I_{s,d}(s) \right). \end{aligned} \tag{3.3}$$

By substituting $V_{t,x}(s) = m_{s,x}(\frac{V_{dc}}{2})$ into (3.3), in which $x \in \{d,q\}$, the following expressions are obtained for the currents synthesized by the ES-STATCOM(PAULO, 2023):

$$\begin{aligned} I_{s,d}(s) &= \frac{1}{sL_{eq} + R_{eq}} \left[m_{s,d}(s) \left(\frac{V_{dc}}{2} \right) - V_{pcc,d}(s) + \omega L_{eq} I_{s,q}(s) \right], \\ I_{s,q}(s) &= \frac{1}{sL_{eq} + R_{eq}} \left[m_{s,q}(s) \left(\frac{V_{dc}}{2} \right) - V_{pcc,q}(s) - \omega L_{eq} I_{s,d}(s) \right], \end{aligned} \tag{3.4}$$

in which $m_{s,x}(s)$ are the modulation index in the dq coordinates, and V_{dc} is the dc bus voltage of the ES-STATCOM.

3.1 CONTROL STRATEGIES

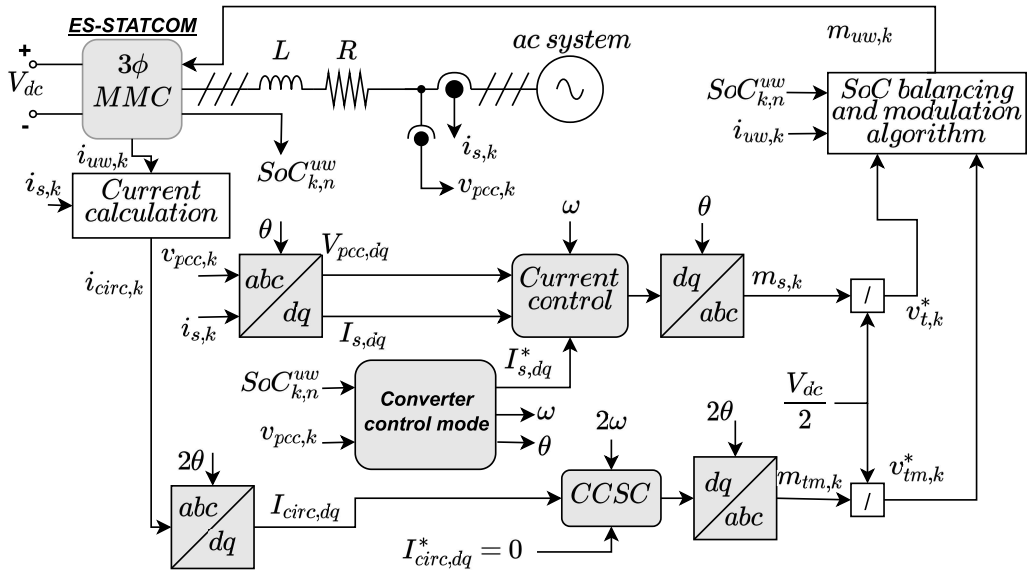
The complete control system implemented in this work is presented in this section, where Figure 11 illustrates the full control structure of the ES-STATCOM. It is worth noting that the currents in the upper and lower arms of each phase are measured, denoted respectively as $i_{u,k}$ and $i_{w,k}$; and also the currents $i_{s,k}$; the voltages $v_{pcc,k}$; and the $SoC^{uw}_{k,n}$, which refer to the n^{th} SoC of the upper (^{u}) or lower (^{w}) SM of phase k, in which $n \in \{1,\ldots,N\}$ and $k \in \{a,b,c\}$. Additionally, the current controller, the CCSC, and the converter control mode blocks are shown, all of which are described in more detail in the following subsections.

3.1.1 Control of the output currents of the ES-STATCOM

The expressions given in (3.4) can be used to design two control loops for the ES-STATCOM. Since $I_{s,d}(s)$ and $I_{s,q}(s)$ exhibit steady-state characteristics in the dq coordinate system, proporcional-integral (PI) controllers can be designed to ensure that the output currents of the ES-STATCOM follow reference signals with zero steady-state error.

The control strategy adopted in this work is achieved by modifying the modulation indices. Thus, by controlling $m_{s,d}$ and $m_{s,q}$, the output voltages of the converter are adjusted, thereby regulating the synthesized currents.

Figure 11 – Control structure of the ES-STATCOM.



Source: Prepared by the author (2025).

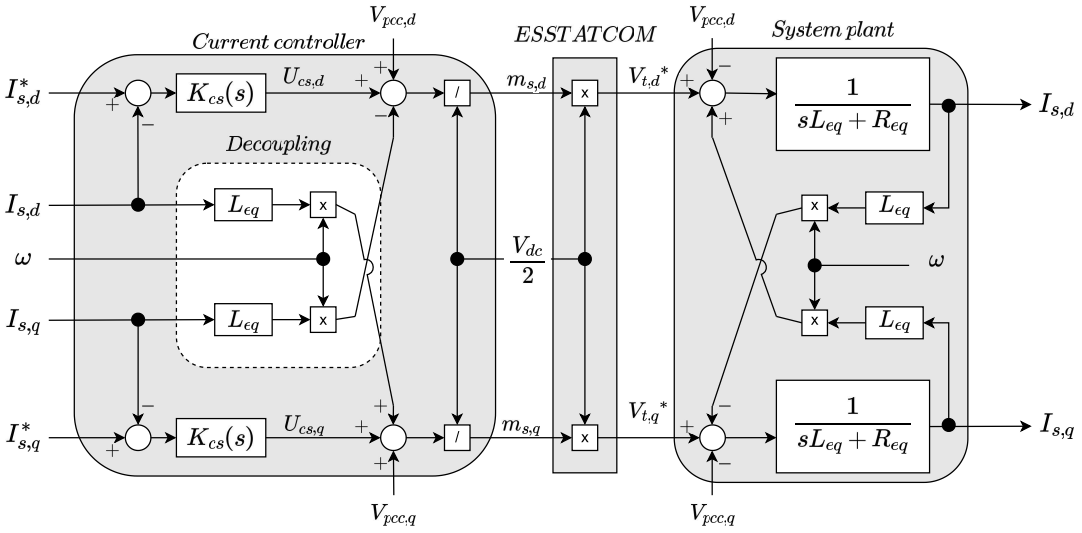
By defining two new control variables in the d and q coordinates as $U_{cs,d}(s)$ and $U_{cs,q}(s)$, the following control functions can be written:

$$\begin{aligned} m_{s,d}(s) &= \frac{2}{V_{dc}}(U_{cs,d}(s) + V_{pcc,d}(s) - \omega L_{eq} I_{s,q}(s)), \\ m_{s,q}(s) &= \frac{2}{V_{dc}}(U_{cs,q}(s) + V_{pcc,q}(s) + \omega L_{eq} I_{s,d}(s)). \end{aligned} \tag{3.5}$$

Based on (3.4) and (3.5), the block diagram shown in Figure 12 can be drawn. The errors between the reference currents and the output currents in the d and q coordinates are processed by two controllers $K_{cs}(s)$, whose output signals are combined with the feed-forward voltage and decoupling signals, resulting in the control signals $U_{cs,d}(s)$ and $U_{cs,q}(s)$. These signals, in turn, are normalized with respect to half of the dc bus voltage, yielding the modulation indices $m_{s,d}(s)$ and $m_{s,q}(s)$, which are used to generate the switching signals for the converter's power switches.

The PI controllers in Figure 12 are responsible for adjusting the converter's terminal voltage in order to maintain the desired current levels, even in the presence of disturbances or variations in the reference signals. While the feed-forward loop ensures robustness of the controller against disturbances caused by grid voltage fluctuations, the decoupling loop is responsible for separating and eliminating any mutual interference between the currents in the direct and quadrature axes. In this way, the control loops can be designed independently, without one affecting the other.

Figure 12 – ES-STATCOM outputs current control loop.



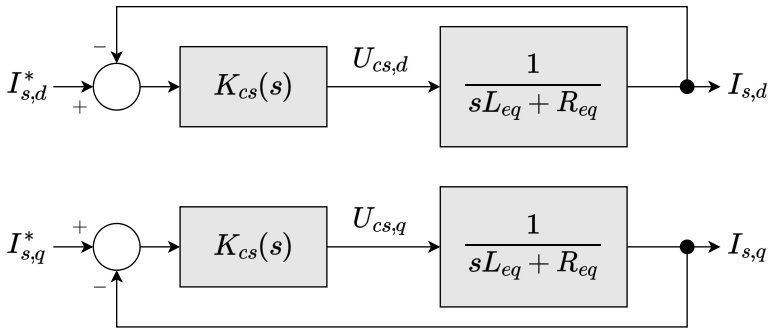
Source: Prepared by the author (2025).

Substituting (3.5) into (3.4) yields:

$$\begin{aligned} I_{s,d}(s) &= \frac{1}{sL_{eq}+R_{eq}}U_{cs,d}(s), \\ I_{s,q}(s) &= \frac{1}{sL_{eq}+R_{eq}}U_{cs,q}(s). \end{aligned} \tag{3.6}$$

From (3.6), the simplified block diagram illustrated in Figure 13 can be drawn. It can be observed in this figure that the currents in the d and q coordinates depend solely on the control variables in their respective coordinates and on the equivalent impedance of the interface filter between the ES-STATCOM and the power grid.

Figure 13 – Simplified block diagram of the ES-STATCOM outputs current control loop.



Source: Prepared by the author (2025).

Based on the block diagrams shown in Figure 13, the following expressions can be written for the closed-loop transfer functions in the d and q coordinates for the

ES-STATCOM:

$$G_{cs,dq}(s) = \frac{I_{s,dq}(s)}{I^*_{dq}(s)} = \frac{\frac{1}{L_{eq}}\left(sk_{p,cs} + k_{i,cs}\right)}{s^2 + s\left(\frac{k_{p,cs}+R_{eq}}{L_{eq}}\right) + \left(\frac{k_{i,cs}}{L_{eq}}\right)} \ , \tag{3.7}$$

in which $k_{p,cs}$ and $k_{i,cs}$ are the proportional and integral gains, respectively, of the controller K_{cs}, being $K_{cs} = (k_{p,cs} + k_{i,cs}/s)$.

By comparing the denominator of (3.7) with the canonical form of a second-order system, the proportional and integral gains can be designed as:

$$k_{p,cs} = 2\zeta_{cs}\omega_{cs}L_{eq} - R_{eq} \tag{3.8}$$

and,

$$k_{i,cs} = \omega^2_{cs}L_{eq} \ , \tag{3.9}$$

in which ω_{cs} is the undamped natural frequency and ζ_{cs} is the damping factor of the closed-loop transfer function of the current control loop given in (3.7).

3.1.2 **Circulating current suppressing control**

Even after balancing the SoC values and equalizing the output voltages of the SM, energy transfer will still occur between the converter's SM, resulting in a current flow between the arms of the ES-STATCOM. These internal currents, also referred to as circulating currents, primarily consist of oscillating components, which include even harmonic multiples of the fundamental frequency of the ac grid current, with the predominant component being the second harmonic (2ω).

Figure 14 illustrates the equivalent circuit showing the internal currents flowing in each leg of the ES-STATCOM. The currents flowing through the upper and lower arms are composed of three components, as presented below (LI *et al.*, 2013; ALMEIDA *et al.*, 2017; ANGQUIST *et al.*, 2011):

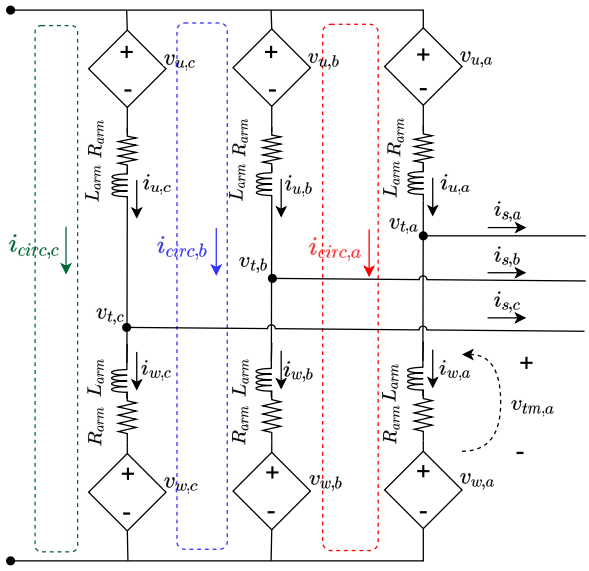
$$\begin{aligned} i_{u,k} &= \frac{1}{3}i_{dc} + \frac{1}{2}i_{s,k} + i_{circ,k} \ , \\ i_{w,k} &= \frac{1}{3}i_{dc} - \frac{1}{2}i_{s,k} + i_{circ,k} \ , \end{aligned} \tag{3.10}$$

in which i_{dc} is the dc component of the current and is zero due to the open circuit on the dc side of the ES-STATCOM, $i_{s,k}$ is the terminal current for each phase, and $i_{circ,k}$ is the ac circulating component flowing through the ES-STATCOM arm in each phase.

Considering the direction of the currents and the voltage polarities indicated in Figure 14, the following relations can be written for the upper and lower arms of the ES-STATCOM:

$$\begin{aligned} \frac{V_{dc}}{2} - v_{u,k} - v_{t,k} &= R_{arm}i_{u,k} + L_{arm}\frac{di_{u,k}}{dt} \ , \\ \frac{V_{dc}}{2} - v_{w,k} + v_{t,k} &= R_{arm}i_{w,k} + L_{arm}\frac{di_{w,k}}{dt} \ , \end{aligned} \tag{3.11}$$

Figure 14 – Equivalent circuit illustrating current flow within the ES-STATCOM.



Source: Prepared by the author (2025).

in which $v_{u,k}$ and $v_{w,k}$ are the voltages of the upper and lower arms, respectively, and $v_{t,k}$ is the terminal voltage of each ES-STATCOM phase.

By adding the expressions in (3.10), and substituting the result into the sum of the expressions in (3.11), the following expression is obtained:

$$\frac{V_{dc}}{2} - \frac{(v_{u,k} + v_{w,k})}{2} = R_{arm} i_{circ,k} + L_{arm} \frac{di_{circ,k}}{dt} \ . \tag{3.12}$$

From (3.12), the circulating current depends on the voltage imbalance defined for each ES-STATCOM leg as follows:

$$v_{tm,k} = R_{arm} i_{circ,k} + L_{arm} \frac{di_{circ,k}}{dt} \ . \tag{3.13}$$

The control of the voltage $v_{tm,k}$ can then be used to mitigate the circulating currents. From (3.12) and (3.13), auxiliary expressions for the reference voltages of the upper and lower arms are obtained as follows:

$$\begin{aligned} v_{u,k} &= \frac{V_{dc}}{2} - v_{t,k} - v_{tm,k} \ , \\ v_{w,k} &= \frac{V_{dc}}{2} + v_{t,k} - v_{tm,k} \ . \end{aligned} \tag{3.14}$$

Considering that the modulation indices of the upper and lower arms of each ES-STATCOM phase are, respectively, $m_{u,k} = (v_{u,k}/V_{dc})$ and $m_{w,k} = (v_{w,k}/V_{dc})$; that the modulation index due to the imbalance voltage is $m_{tm,k} = (v_{tm,k}/V_{dc})$; and that the modulation index of the terminal voltage is $m_{s,k} = (2v_{t,k}/V_{dc})$, the following relations can

be written for the upper and lower arms of each ES-STATCOM leg:

$$\begin{aligned} m_{u,k} &= \frac{1}{2}(1 - m_{s,k}) - m_{tm,k} \ , \\ m_{w,k} &= \frac{1}{2}(1 + m_{s,k}) - m_{tm,k} \ . \end{aligned} \tag{3.15}$$

Although the internal currents do not directly affect the ac currents synthesized by the ES-STATCOM, their presence increases the root mean square (RMS) value of the currents in the converter arms, leading to additional losses and a reduction in overall efficiency. Therefore, it is crucial to compensate for these currents to prevent the over-sizing of the converter components (DU *et al.*, 2017).

In order to ensure the total compensation of the circulating currents through the converter arms, the direct control technique or CCSC can be used. Therefore, the circulating currents in the ES-STATCOM arms, which are predominantly second-order and negative-sequence components, are measured and transformed into the $d-q$ coordinate system with an angular frequency of 2ω. Subsequently, PI controllers process the errors between the measured currents and their reference values, providing the imbalance voltages that the converter arms must synthesize.

Following the same methodological steps presented in Subsection 3.1.1 for the control of the three-phase currents synthesized by the ES-STATCOM, the Park transformation in (3.13) can be applied, considering that $\theta = 2\omega t$, yielding:

$$\begin{aligned} v_{tm,d} &= R_{arm} i_{circ,d} + L_{arm} \frac{di_{circ,d}}{dt} + 2\omega L_{arm} i_{circ,q} \ , \\ v_{tm,q} &= R_{arm} i_{circ,q} + L_{arm} \frac{di_{circ,q}}{dt} - 2\omega L_{arm} i_{circ,d} \ . \end{aligned} \tag{3.16}$$

Now, by applying the Laplace transform to (3.16), the following can be written:

$$\begin{aligned} V_{tm,d}(s) &= I_{circ,d}(s)(R_{arm} + sL_{arm}) + 2\omega L_{arm} I_{circ,q}(s), \\ V_{tm,q}(s) &= I_{circ,q}(s)(R_{arm} + sL_{arm}) - 2\omega L_{arm} I_{circ,d}(s). \end{aligned} \tag{3.17}$$

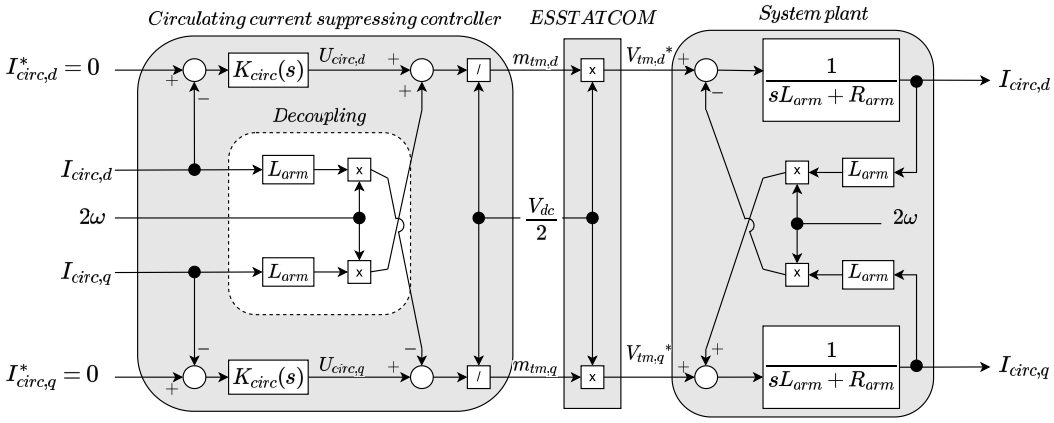
By normalizing (3.17) with respect to V_{dc}, and repeating the procedure followed in the previous subsection with the output current control loop, the following control functions can be written to regulate the circulating currents through the converter arms:

$$\begin{aligned} m_{tm,d} &= \frac{2}{V_{dc}}(U_{circ,d}(s) + 2\omega L_{arm} I_{circ,q}(s)), \\ m_{tm,q} &= \frac{2}{V_{dc}}(U_{circ,q}(s) - 2\omega L_{arm} I_{circ,d}(s)), \end{aligned} \tag{3.18}$$

in which $U_{circ,d}(s)$ and $U_{circ,q}(s)$ are the control variables.

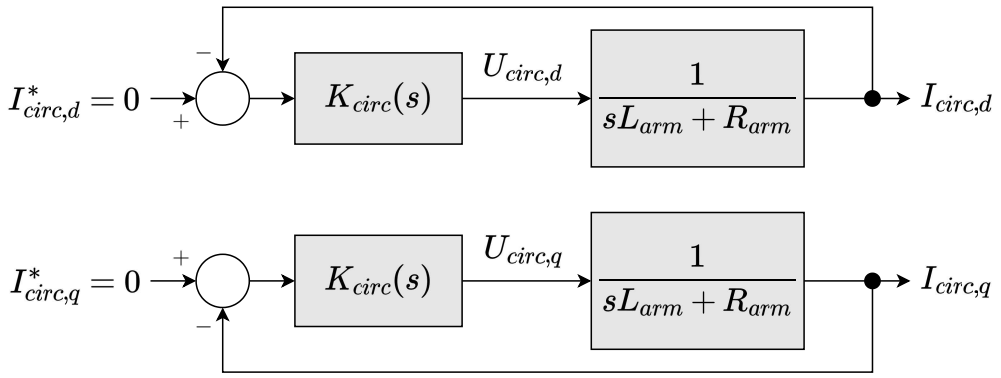
Now, with (3.17) and (3.18) in hand, the block diagram shown in Figure 15 can be drawn, and the decoupled loops to mitigate the circulating currents, as shown in the block diagram of Figure 16, can be derived.

Figure 15 – Circulating current control loop.



Source: Prepared by the author (2025).

Figure 16 – Simplified block diagram of the circulating current control loop.



Source: Prepared by the author (2025).

It is noted that the reference currents in the d and q coordinates are zero, since the ultimate goal is to cancel these currents. Thus, from the decoupled circulating current control block diagram, the following equations can be obtained:

$$\begin{aligned} I_{circ,d}(s) &= \frac{1}{sL_{arm}+R_{arm}} U_{circ,d}(s), \\ I_{circ,q}(s) &= \frac{1}{sL_{arm}+R_{arm}} U_{circ,q}(s). \end{aligned} \tag{3.19}$$

Now, the following closed-loop transfer functions for the block diagram in Figure 16 can be determined, where the controller $K_{circ}(s)$ is a PI controller, and $k_{circ,p}$ and $k_{circ,i}$ are its proportional and integral gains, respectively:

$$G_{circ,dq}(s) = \frac{I_{circ,dq}(s)}{I^*_{circ,dq}(s)} = \frac{\frac{1}{L_{arm}}\left(sk_{circ,p}+k_{circ,i}\right)}{s^2 + s\left(\frac{k_{circ,p}+R_{arm}}{L_{arm}}\right) + \left(\frac{k_{circ,i}}{L_{arm}}\right)} \quad . \tag{3.20}$$

Finally, by comparing the denominator of the transfer function given in expression (3.20) with the canonical form of a second-order system, the proportional and integral gains of the controller can be designed as follows:

$$k_{circ,p} = 2\zeta_{circ}\omega_{circ}L_{arm} - R_{arm} \tag{3.21}$$

and,

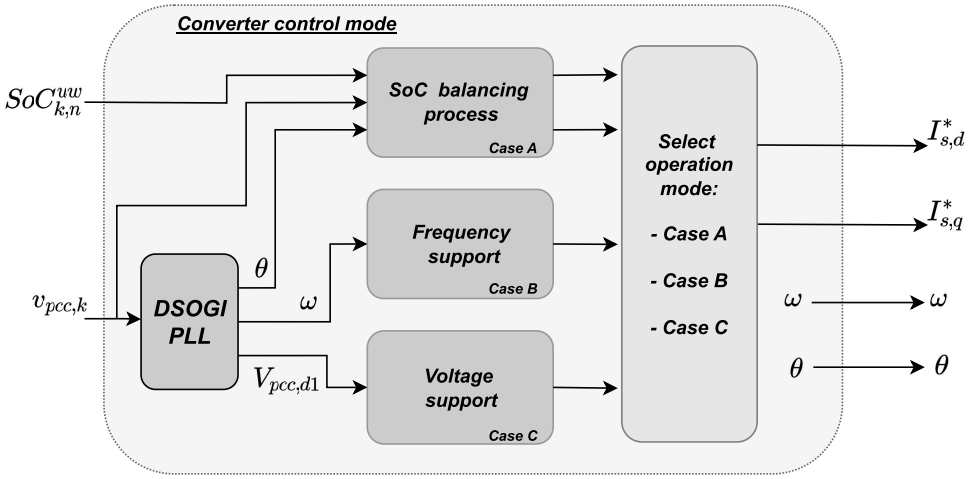
$$k_{circ,i} = \omega_{circ}^2 L_{arm} \ , \tag{3.22}$$

in which ω_{circ} is the undamped natural frequency and ζ_{circ} is the damping factor of the closed-loop transfer function of the circulating current control through the ES-STATCOM arm.

3.1.3 Converter control mode

Figure 17 illustrates the converter control mode block shown in Figure 11. It allows the selection of the three possible ES-STATCOM operating cases, namely Case A, Case B, and Case C, corresponding respectively to the SoC balancing process, frequency support, and voltage support. The first case occurs under normal network operating conditions, whereas the other two are triggered under special circumstances, such as the connection of a large load or a system fault. Each case operates in a non-simultaneous manner, and the reference current signals $I_{s,d}^*$ and $I_{s,q}^*$ are defined differently for each one, as explained below. The positive-sequence voltage at the direct axis of the PCC, $V_{pcc,d1}$, which is required for voltage support, is provided through the DSOGI method (Appendix B).

Figure 17 – Converter control mode scheme.



Source: Prepared by the author (2025).

3.1.3.1 *SoC balancing proccess*

For Case A, there are two options to perform the SoC balancing process, as illustrated in Figure 18. In the first option, i.e., Case A.1, the current references can be defined based on the instantaneous active and/or reactive power values set as references. As long as there is current flowing through the arms of the ES-STATCOM, SoC balancing can be achieved by synthesizing both active and reactive currents at the converter terminals, thus the power references can be applied either simultaneously or individually, that is, with both being nonzero at the same time, or with one being nonzero and the other equal to zero.

Based on Akagi, Watanabe e Aredes (2017), the following matrix relation can be written for the active (p_s) and reactive (q_s) powers, in synchronous reference frame, at the terminals of the ES-STATCOM:

$$\begin{bmatrix} p_s \\ q_s \end{bmatrix} = \begin{bmatrix} v_{pcc,d} & v_{pcc,q} \\ v_{pcc,q} & -v_{pcc,d} \end{bmatrix} \begin{bmatrix} i_{s,d} \\ i_{s,q} \end{bmatrix}, \tag{3.23}$$

in which $v_{pcc,d}$ and $v_{pcc,q}$ are the d-axis and q-axis components of the voltage at the PCC, respectively, $i_{s,d}$ and $i_{s,q}$ are the d-axis and q-axis components of the current synthesized by the ES-STATCOM, both represented in the synchronous dq reference frame.

Considering that the angle θ, tracked by the DSOGI-PLL (Appendix B) and used in the Park transformation, aligns the q-axis of the synchronous reference frame with the PCC voltage space vector, (3.23) can be reduced to,

$$\begin{bmatrix} p_s \\ q_s \end{bmatrix} = \begin{bmatrix} 0 & V_{pcc} \\ V_{pcc} & 0 \end{bmatrix} \begin{bmatrix} i_{s,d} \\ i_{s,q} \end{bmatrix}, \tag{3.24}$$

in which $v_{pcc,d} = 0$ and $v_{pcc,q} = V_{pcc}$, with V_{pcc} being the amplitude of the voltage space vector at PCC.

Therefore, using (3.24) in its inverse form, the q-axis current component $i_{s,q}$ can be used to control the active power, while the d-axis current component $i_{s,d}$ can be used to control the reactive power at the ES-STATCOM, as shown below:

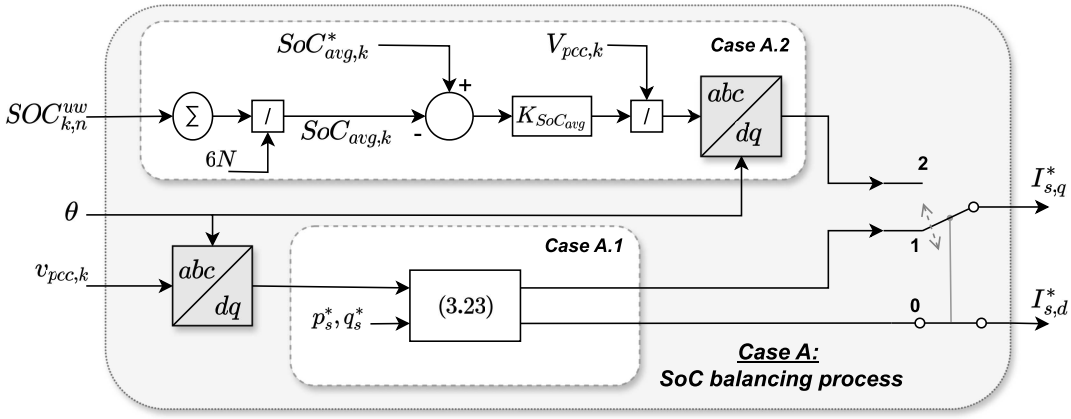
$$\begin{cases} i^*_{s,q} = \left(\dfrac{1}{V_{pcc}}\right) p^*_s \\ i^*_{s,d} = \left(\dfrac{1}{V_{pcc}}\right) q^*_s \end{cases}, \tag{3.25}$$

in which p^*_s and q^*_s are, respectively, the reference instantaneous active and reactive powers set for the ES-STATCOM.

It is also important to note that, in this sub-case, the interlocking switch is closed at positions 0 and 1. Additionally, in Case A.1, the SoC balancing is carried out up to the time instant at which the N SoC values converge around their average value, which results

in random final convergence values of the SoC due to characteristics of the balancing algorithm employed.

Figure 18 – SoC balancing process schemes.



Source: Prepared by the author (2025).

The second option in Case A constitutes a refinement of Case A.1, under the condition that the SoC balancing is achieved exclusively through active power. It's refers to the SoC balancing process through global SoC control, defined as Case A.2 in Figure 18. In this sub-case, it is necessary to use the estimated SoC values of each SM in the converter. From these, the average SoC for each leg of the ES-STATCOM $SoC_{avg,k}$ is calculated and compared to a predefined reference value $SoC^*_{avg,k}$. The resulting error is processed by a PI controller, and after being divided by the RMS voltage at the PCC, the required current reference for SoC balancing is determined. In this condition, the interlocking switch is closed at position 2, while positions 0 and 1 remain opened, meaning that only $I^*_{s,q}$ is provided.

In order to achieve global SoC balancing among the legs of the ES-STATCOM, a centralized PI controller is proposed. The SoC error of leg k with respect to the average SoC is defined as:

$$\Delta SoC_{avg,k}(t) = SoC^*_{avg,k} - SoC_{avg,k} \ . \tag{3.26}$$

The SoC dynamics are directly influenced by the active power exchanged with each leg, then:

$$\frac{dSoC_{avg,k}(t)}{dt} = -\frac{p_k(t)}{E_k} \ , \tag{3.27}$$

in which $p_k(t)$ is the instantaneous active power associated with leg k and E_k is its corresponding energy capacity (in MWh).

To eliminate the SoC deviation, a reference power signal is generated using a PI controller:

$$p^*_k(t) = k_{p,SoC_{avg}} \Delta SoC_{avg,k}(t) + k_{i,SoC_{avg}} \int_0^t \Delta SoC_{avg,k}(t)\, dt \ , \tag{3.28}$$

in which $k_{p,SoC_{avg}}$ and $k_{i,SoC_{avg}}$ are the proportional and integral gains of the PI controller $K_{SoC_{avg}}(s)$, respectively, and are expressed in MW per unit of SoC.

The reference current to be injected by each leg is obtained by dividing the reference power by the RMS voltage at the PCC:

$$i_k^*(t) = \frac{p_k^*(t)}{V_{pcc,k}} = \frac{1}{V_{pcc,k}} \left[k_{p,SoC_{avg}} \Delta SoC_{avg,k}(t) + k_{i,SoC_{avg}} \int_0^t \Delta SoC_{avg,k}(t)\, dt \right]. \quad (3.29)$$

This current reference is transformed to the SRF, and subsequently only its q-component is used as the reference in the output current control loop. Based on this approach, the global SoC control loop shown in Figure 18 can be constructed.

It is important to emphasize that in this improvement of Case A.1 under the condition of SoC balancing exclusively through active power, as observed, it is possible to set the N balanced SoC values to a predefined target specified by the system operator.

3.1.3.2 *Ancillary services cases*

The controls in cases B and C are for when there is a disturbance in the system. Under these conditions, the ES-STATCOM has the capacity to provide ancillary services. Thus, two operating conditions of the grid will be considered, such as, the entry of a large load and the occurrence of a fault.

In scenarios where a large load is suddenly connected or disconnected, the system frequency tends to deviate from the nominal value. The ES-STATCOM can provide primary frequency support by adjusting its output current proportionally to the frequency deviation.

The frequency deviation is defined as:

$$\Delta\omega(t) = \omega^* - \omega(t), \quad (3.30)$$

in which ω^* is the nominal angular frequency, and $\omega(t)$ is the measured grid angular frequency.

This deviation is used as input to a PI controller, which directly generates the current reference in the SRF, related to the instantaneous active power:

$$i_{s,q}^*(t) = k_{p,\omega} \Delta\omega(t) + k_{i,\omega} \int_0^t \Delta\omega(t)\, dt\ , \quad (3.31)$$

in which $k_{p,\omega}$ and $k_{i,\omega}$, are respectively, the proportional and integral gains of the PI controller $K_\omega(s)$.

In the event of a grid fault or voltage sag, the ES-STATCOM contributes to voltage recovery by injecting reactive current based on the positive-sequence voltage magnitude at the PCC.

The voltage deviation is defined as:

$$\Delta v_{pcc,d1}(t) = V^*_{pcc,d1} - v_{pcc,d1}(t), \tag{3.32}$$

in which $V^*_{pcc,d1}$ is the nominal voltage required, and $v_{pcc,d1}(t)$ is the direct-axis component of the positive-sequence voltage magnitude at the PCC.

This voltage deviation is also fed into a PI controller that directly generates the current reference in the SRF, related to the instantaneous reactive power:

$$i^*_{s,d}(t) = k_{p,V_{pcc}} \Delta v_{pcc,d1}(t) + k_{i,V_{pcc}} \int_0^t \Delta v_{pcc,d1}(t)\, dt \ , \tag{3.33}$$

in which $k_{p,V_{pcc}}$ and $k_{i,V_{pcc}}$, are respectively, the proportional and integral gains of the PI controller $K_{V_{pcc}}(s)$.

Figure 19 – Ancillary services cases schemes.

(a) (b)

Caption: (a) Block diagram of frequency support; (b) Block diagram of voltage support.

Source: Prepared by the author (2025).

These control strategies ensure that the ES-STATCOM dynamically contributes to the stabilization of both frequency and voltage. Based on the equations above, the corresponding control loops, shown in Figure 19(a) and Figure 19(b), can be constructed to provide ancillary services in response to system disturbances.

It is important to emphasize that, in a practical power system, maintaining frequency and voltage strictly at their nominal values would require the batteries system to possess an extremely large storage capacity. Therefore, in real applications, the reference values of frequency and voltage are typically adjusted through a droop-based control strategy (JÚNIOR, 2024).

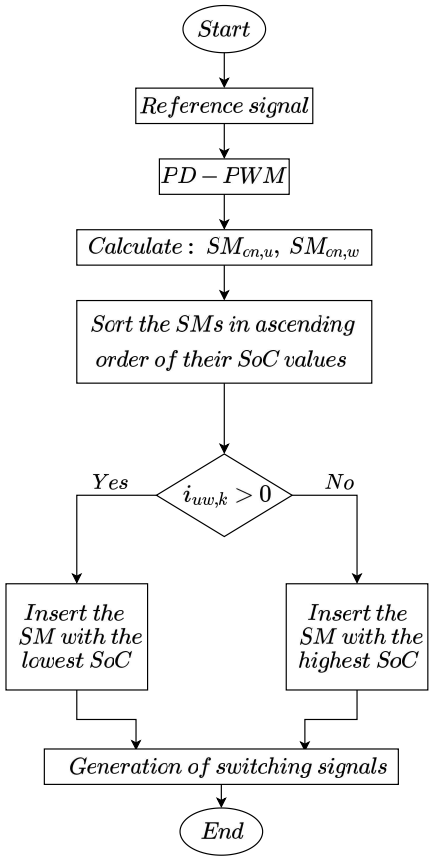
3.1.4 **SoC balancing algorithm**

Starting from the premise that each cell and battery pack has been previously regulated by the BMS, and that each battery rack connected to each SM has different initial voltage and SoC values, it is necessary to employ a balancing method between the submodules to prevent the SoC difference from increasing over time. As discussed in the previous chapters, if the SoC difference between the SM becomes too large, the available

capacity will be significantly reduced because the fuller battery restricts the maximum charge, while the emptier battery limits the minimum charge. Therefore, the balancing strategy adopted in this work aligns with the characteristics of Non-Dissipative balancing methods performed online with the grid (NAGUIB; KOLLMEYER; EMADI, 2021).

In Figure 20, the structure of the algorithm for SoC balancing is presented, along with the modulation of the ES-STATCOM. Initially, PD-PWM modulation with N multi-carriers is performed using the sinusoidal reference signals $v_{u,k}$ and $v_{w,k}$ given by (3.14). These references, when compared with the multi-carriers, result in the number of SM that should be inserted in each arm, $SM_{on,u}$ and $SM_{on,w}$, at each instant in time.

Figure 20 – Flowchart of the SoC balancing algorithm.



Source: Prepared by the author (2025).

Subsequently, after measuring the N values of SoC and the number of SM to be inserted in each arm, a sorting from the smallest to the largest SoC value is performed using the bubble sort method. After this sorting, depending on the direction of the current circulating through the arm, the submodules to be inserted or bypassed are selected, charging or discharging its battery rack corresponding SoC, respectively. Each of the N SoC values is compared to their mean value ($\frac{1}{N}\sum_{n=1}^{N} SoC_{k,n}^{uw}$), which causes them to

gradually converge toward this average over time. This process ensures that deviations from the mean are corrected with each control iteration, promoting uniform charge distribution across the submodules.

Finally, switching signals are generated for the bidirectional self-commutated semiconductor switches of the converter. After the loop is repeated for a certain amount of time, the SoC values become fully balanced, converging around the average value of the SoC in the arm, thus enabling the efficient performance of the ES-STATCOM in providing ancillary services. Further details of this sorting strategy applied to modular multilevel converters, as well as a more in-depth explanation of the bubble sort method, can be found in Ghetti (2019).

3.1.5 **Battery rack electrical performance model**

As presented in the previous chapter, the lithium-ion battery (SLPB120216216 from Kokam) was considered and simulated by Electrical Performance (EP) model (VASILADIOTIS; RUFER, 2014; LI *et al.*, 2017; CAO; KROEZE; KREIN, 2016).The EP model was implemented in the software PLECS [1] exclusively to obtain the open-circuit voltage versus SoC data of the battery, in order to use this information in the ES-STATCOM simulation carried out in PSCAD/EMTDC.

Figure 21 shows the battery rack model based on the EP model employed in this work (ANTON *et al.*, 2013). This aggregated model calculates the current and voltage of the battery rack. A notable feature of this model is that its complexity is independent of the number of series-connected battery packs (N_s) per string and the number of parallel strings (N_p). Additionally, this model provides an estimate of the equivalent SoC of the battery rack based on the SoC estimation approach proposed by Fotouhi *et al.* (2016):

$$SoC(t) = \frac{1}{C_{bat}} \int_0^t i_{bat}(t)\, dt + SoC_0 \ , \tag{3.34}$$

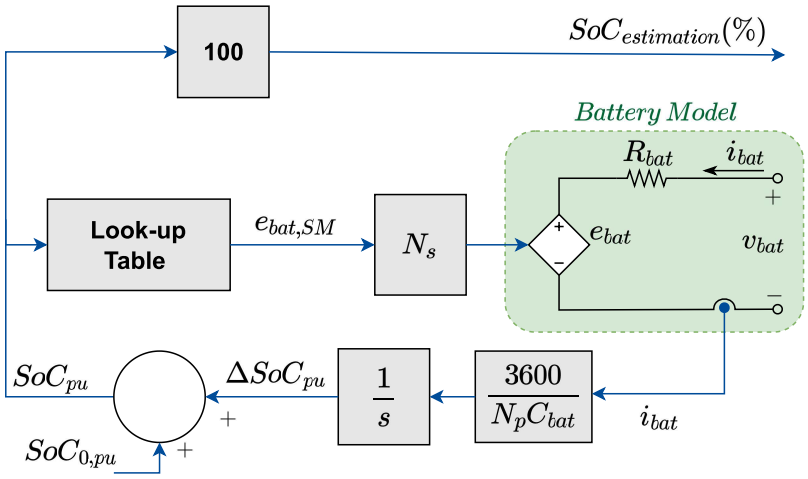
in which C_{bat} is the nominal capacity of the battery, SoC_0 is the initial SoC at the beginning of the analyzed cycle, and i_{bat} is the instantaneous battery current.

This model is defined with the following characteristics, adopted to simplify the study: the battery is represented by a controlled voltage source in series with a resistor. The controlled source represents the open-circuit voltage or no-load voltage (e_{bat}) of the battery, while the resistor R_{bat} models the internal losses, as illustrated in Figure 21. It is important to note that the gains $\frac{1}{N_p C_{bat}}$ and N_s represent the scaling from the battery pack to the battery rack, and the factor 3600 corresponds to the number of seconds in one hour, representing the time basis for battery energy exchange calculations.

An electrical resistance of 0.9 mΩ at 23 °C is assumed, based on the impedance magnitude provided in the *datasheet* (Kokam, 2019). Additionally, the resistance exhibits

[1] The PLECS software was used to consider the thermal effects on the battery resistance.

Figure 21 – Structure of the battery rack model.



Source: Prepared by the author (2025).

linear behavior with temperature, increasing by 10% at 33 °C. The resistance value is limited to a minimum of 0.01 mΩ and a maximum of 10 mΩ.

The considered model is developed based only on the discharge curves of the battery. It is assumed that the charging behavior follows the same open-circuit characteristics, i.e., hysteresis is neglected. Discharge data under different C_{rate} and temperatures were extracted from Kokam (2019) using the software *WebPlotDigitizer*. After data collection, and considering that the voltage values from Kokam (2019) correspond to the terminal voltage v_{bat}, the non-load voltage e_{bat} was calculated as:

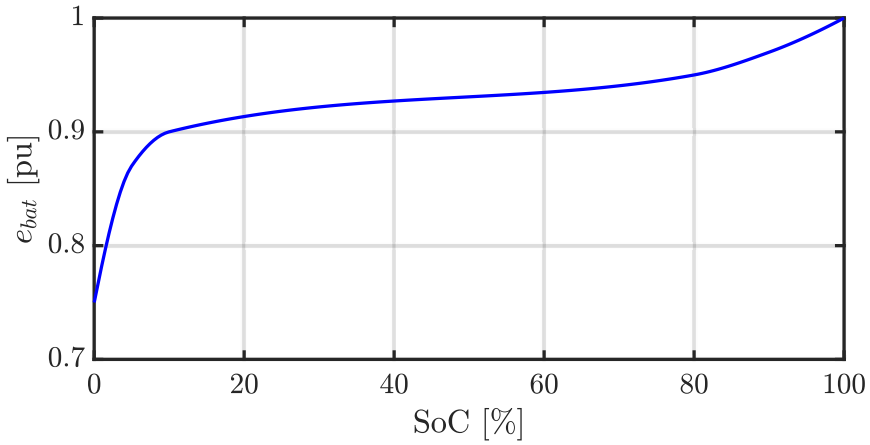
$$e_{bat} = v_{bat} + N_p C_{bat} C_{rate} R_{bat} \ , \tag{3.35}$$

in which C_{bat} is equal to 53 Ah, and C_{rate} is the discharge rate of the battery.

Once e_{bat} values were computed for each temperature and C_{rate}, the SoC was used as the horizontal axis to simplify the implementation of this data in PLECS. For this, a MATLAB function was developed to interpolate the curves. Then, the characteristic discharge curve of the implemented battery, shown in Figure 22, is included through a look-up table of the Figure 21. Additionally, the curve shown in Figure 22 presents a behavior similar to the results from practical tests on Lithium-ion batteries carried out by Meng *et al.* (2017).

Once the battery discharge characteristic curve is obtained, the simplified battery rack model can be implemented in the HBSM of the ES-STATCOM within PSCAD/EMTDC as shown in Figure 8, where, for simplicity, the internal resistance of the battery rack model is considered constant and only the vectors with the open-circuit voltage and SoC values provided by the battery characteristic curve are given as data for the simulations. This input data for the battery rack model adopted, was considered as ten points of the

Figure 22 – Discharge characteristic curve of the Lithium-ion battery.



Source: Prepared by the author (2025).

curve illustrated in Figure 22, in Table 6 is possible to observe those points used in the PSCAD/EMTDC simulations.

Table 6 – Simulation data corresponding to the battery characteristic curve.

Point	SoC [%]	e_{bat} [pu]
1	100.0000	1.0000
2	88.5572	0.9665
3	77.6119	0.9473
4	66.6667	0.9382
5	55.7214	0.9328
6	44.2786	0.9287
7	33.3333	0.9239
8	22.3881	0.9159
9	11.4428	0.9023
10	0.0010	0.7500

Source: Prepared by the author (2025).

3.2 ES-STATCOM PARAMETERS SETTING

To ensure the proper operation of an ES-STATCOM, the minimum required dc-link voltage, considering the injection of 1 pu of reactive current, PCC voltage variation, and the voltage drop across the equivalent output impedance, is expressed as (FUJII; SCHWARZER; DONCKER, 2005; CUPERTINO *et al.*, 2018):

$$V_{dc,min} = \frac{2\sqrt{2}}{m_{max}\sqrt{3}} V_{pcc} \left(1 + \Delta V_{pcc} + X_{eq}\right), \tag{3.36}$$

in which V_{pcc} represents the RMS line-to-line PCC voltage, ΔV_{pcc} is the maximum anticipated PCC voltage variation (in pu), m_{max} denotes the maximum modulation index, and

X_{eq} is the per-unit equivalent output reactance of the converter, given by:

$$X_{eq} = \left(X + \frac{X_{arm}}{2} \right), \tag{3.37}$$

in which X_{arm} and X are the per-unit arm reactance and the reactance on the grid-side, respectively.

Equation (3.36) describes the scenario for capacitive operation, which requires the converter to generate a terminal voltage higher than the grid voltage. This higher voltage compensates for both the PCC voltage and the voltage drop across the output inductance, disregarding the effects of arm and interface filter resistances. Additionally, the modulation index is inversely related to the minimum dc-link voltage required.

The total voltage of each SM of the ES-STATCOM depends directly on the number of battery packs connected in series. In Figure 22 is possible to see the considerable variation in the battery voltage over the SoC range, this characteristic must be taken into account in this approach. Then, according to AMORIM (2019) the required number of series-connected battery packs is calculated as:

$$N_s = \text{floor} \left(\frac{v_{SM}^*}{v_{bat,max}} \right), \tag{3.38}$$

in which floor$(\cdot)$ is a function that denotes the greatest integer less than or equal to its argument, v_{SM}^* is the nominal SM voltage, and $v_{\text{bat,max}}$ is the maximum voltage of a single battery pack. The use of the floor function ensures that N_s is rounded and selected so the resulting voltage does not exceed the nominal SM voltage.

The total number of SM required per arm is determined by ensuring that the converter is capable of generating the desired output voltage, even under minimum voltage conditions. This calculation takes into account the minimum dc-link voltage and the lowest possible battery rack voltage, and is expressed as:

$$N = \text{ceil} \left(\frac{V_{dc,min}}{N_s v_{bat,min}} \right), \tag{3.39}$$

in which ceil$(\cdot)$ is a function that denotes the smallest integer greater than or equal to its argument, $v_{\text{bat,min}}$ is the minimum voltage of the battery pack, and N_s is the number of packs connected in series within the SM. The ceil function ensures that the number of submodules is sufficient to synthesize the required output voltage even in the worst-case operating scenario, meaning the minimum output voltage.

The dimensioning of the number of parallel battery strings, denoted by N_p, must satisfy two main design constraints: the ES-STATCOM rated power delivery capability and the total energy storage required for the applications. The first criterion ensures that the battery system can deliver the full rated power of the converter to the grid. It is expressed as:

$$N_{p,P} = \text{ceil} \left(\frac{P}{6 N N_s P_{bat,n_{min}}} \right), \tag{3.40}$$

in which P is the nominal converter power, N is the number of SM per arm, N_s is the number of series-connected battery packs per SM, and $P_{bat,n_{min}}$ is the minimum power available from each battery pack.

The minimum rack power is calculated as:

$$P_{bat,rack_{min}} = N_s v_{bat,min} C_{rate,n} C_{bat,n} \ , \tag{3.41}$$

in which $C_{rate,n}$ is the recommended discharge rate factor, and $C_{bat,n}$ is the nominal capacity of the battery rack.

The second criterion addresses the energy storage capability required for the system's application. It is given by:

$$N_{p,E} = \text{ceil}\left(\frac{100E}{6E_{bat,n}NN_s(SoC_{max} - SoC_{min})}\right), \tag{3.42}$$

in which E is the total energy storage requirement of the system, $E_{bat,n}$ is the nominal energy of a single battery pack, and SoC_{max} and SoC_{min} are the maximum and minimum allowable state of charge values, respectively.

To satisfy both power and energy constraints, the final number of parallel battery strings is defined as:

$$N_p = \max(N_{p,P}, N_{p,E}). \tag{3.43}$$

After setting the battery arrangement, the design of passive components and semiconductors for the ES-STATCOM must be completed. This includes the definition of the SM capacitance, the arm inductance, and the current rating for semiconductor devices such as IGBT and diodes.

The SM capacitance is defined based on an energy storage criterion, according to Cupertino *et al.* (2018), for the worst case for MMC in terms of energy requirements and taking into account the capability curve of the converter, considering 1 *pu* of output current, the maximum value of the required energy storage W is approximately 200 MJ/MVA. This requirement aims to ensure adequate energy buffering within each SM and contributes to voltage stability. Then, the required capacitance is calculated as follow (ILVES *et al.*, 2013; CUPERTINO *et al.*, 2018):

$$C = \frac{2WS}{6000N(v^*_{SM})^2} \ , \tag{3.44}$$

in which S is the rated apparent power of the ES-STATCOM. Additionally, the inclusion of capacitance is beneficial for attenuating low-frequency components in the battery current, thereby improving the overall lifetime of the BESS.

The arm inductance is defined to meet a specified per unit reactance and is calculated based on the maximum PCC voltage and nominal operating frequency. Following

the method outlined in Harnefors *et al.* (2012), the inductance is computed as:

$$L_{arm} = X_{arm} \frac{V_{pcc}^2}{2\pi f S} \ , \tag{3.45}$$

in which f is the nominal grid frequency.

Ensuring the setting of the ES-STATCOM parameters, the maximum current flowing through each arm must be considered to properly specify both the passives elements and the power electronics devices. Assuming balanced conditions and decentralized BESS configuration, the mean circulating current value is zero. As such, the maximum arm current in each phase can be approximated by:

$$\max(i_{arm}) = \frac{\max(i_s)}{2} = \frac{S}{\sqrt{6} V_{pcc}} \ , \tag{3.46}$$

in which i_s is the output current of the converter and i_{arm} is the current flowing in each arm. This expression provides a conservative basis for selecting the current ratings of IGBT and designing the thermal and magnetic properties of the arm inductors.

3.3 CHAPTER REMARKS

The present chapter has provided a detailed analysis of the dynamics of the ES-STATCOM to be implemented in this work. It also presented the modeling of control strategies for both the output currents and the circulating currents. The control of the output currents is especially essential for the effective balancing of the SoC, since by precisely regulating these currents, the system enables coordinated energy exchange among the battery racks and the grid, ensuring the balancing algorithm distributes charge evenly.

Although the circulating currents do not interfere directly with the output currents, they must be fully suppressed in order to improve the overall system efficiency, reduce internal losses, and prevent potential long-term degradation of system components. These two current control loops form the core of the control structure, as they are essential for ensuring that the converter operates properly under the various operating conditions for which it is intended, including scenarios involving rapid load changes and voltage disturbances.

The additional control strategies outlined in the converter control mode serve to provide reference values for the output current control of the ES-STATCOM. Furthermore, the chapter explored in greater depth the SoC balancing algorithm, which, upon receiving sinusoidal reference signals derived from the control loops, generates the appropriate switching pattern for the converter. This mechanism ensures that energy is evenly distributed among the storage elements, thereby maintaining battery health and extending system lifespan, while allowing the system to operate efficiently and meet its intended performance objectives.

Internal details of the ES-STATCOM, such as the battery packs model used, the precise definition of the converter parameters, and key assumptions made during the modeling process, were also thoroughly discussed. These details provide a solid foundation for understanding the practical aspects and limitations of the system, ensuring that the theoretical control strategies are effectively translated into real-world implementation. As such, this chapter is of fundamental importance for both the development and comprehensive understanding of the system that will be implemented and presented in the following chapters, serving as a critical reference point for subsequent simulation analyses and experimental validations.

4 SoC BALANCING SIMULATION CASE

The ES-STATCOM, previously presented in detail along with its control architecture, will be modeled using the electromagnetic transients simulation software PSCAD/EMTDC. This chapter introduces the first of three simulation cases to be addressed—Case A—which pertains to the SoC balancing process of the ES-STATCOM when connected to a balanced ac system. Later, Cases B and C, concerning the provision of frequency and voltage supports by the converter connected to the modified IEEE 14-bus system, respectively, will be presented in Chapter 5.

Table 7 – Parameters of the ES-STATCOM.

Parameter	**Value**
DC-link voltage (V_{dc})	30 kV
AC grid RMS line voltage ($v_{s,k}$)	9.76 kV
Arm inductance (L_{arm})	6.4 mH
Arm resistance (R_{arm})	1.0 mΩ
Equivalent inductance (L_{eq})	6.4 mH
Equivalent resistance (R_{eq})	1.5 mΩ
Number of SM (N)	18
Capacitance of each SM (C)	9900 µF
Switching frequency (f_{sw})	1260Hz
Nominal grid frequency (f)	60Hz

Source: Prepared by the author (2025).

Table 8 – Parameters of the controllers.

Parameter	**Value**
Proportional gain – output current control ($k_{p,cs}$)	10 V/A
Integral gain – output current control ($k_{i,cs}$)	3 V/As
Proportional gain – CCSC loop ($k_{circ,p}$)	12 V/A
Integral gain – CCSC loop ($k_{circ,i}$)	1 V/As
Proportional gain – SoC global control ($k_{p,SoC_{avg}}$)	2.4 MW
Integral gain – SoC global control ($k_{i,SoC_{avg}}$)	1.5 MW/s
Proportional gain – Frequency support ($k_{p,\omega}$)	0.125 As/rad
Integral gain – Frequency support ($k_{i,\omega}$)	1.41 A/rad
Proportional gain – Voltage support ($k_{p,V_{pcc}}$)	0.85 A/V
Integral gain – Voltage support ($k_{i,V_{pcc}}$)	2.95 A/Vs
Sampling frequency (f_{samp})	10 kHz

Source: Prepared by the author (2025).

Table 9 – Technical specifications of the battery pack.

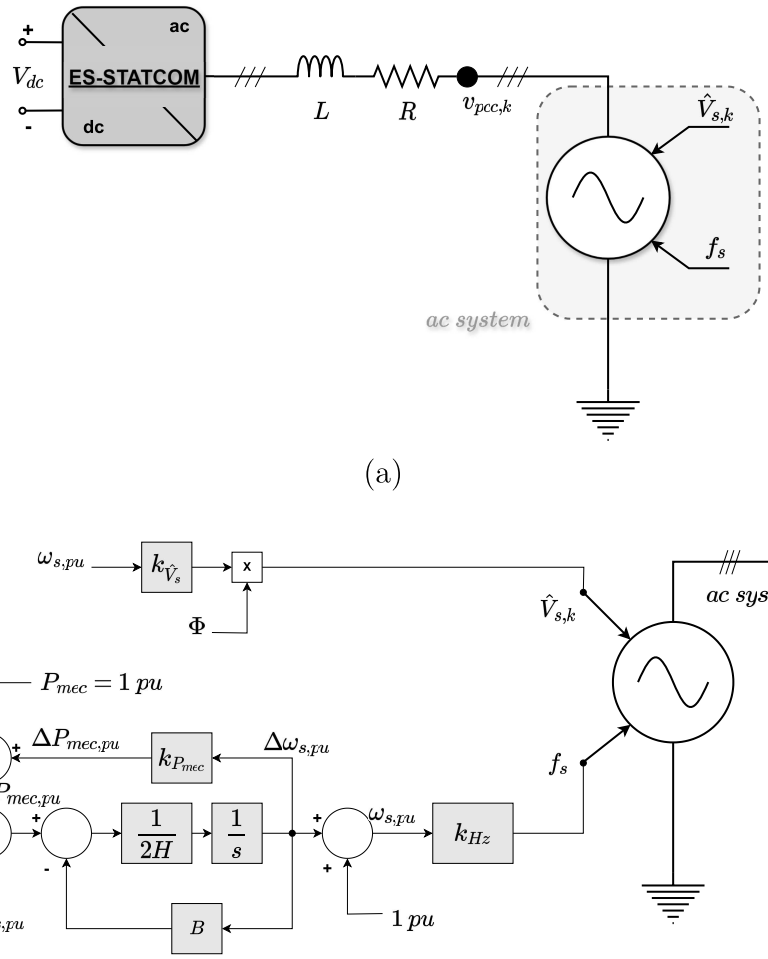
Parameter	**Specification**
Battery pack type	*KBM216 2P 14S*
Battery cell type	*SLPB120216216*
Power capacity (C_{bat})	53 Ah
Discharging rate (C_{rate})	20%
Total energy storage ($E_{bat,n}$)	55kWh
Battery pack minimum voltage ($v_{bat,min}$)	42 V
Battery pack nominal voltage (v_{bat})	51.8 V
Battery pack maximum voltage ($v_{bat,max}$)	58.8 V
Minimum allowed SoC (SoC_{min})	10%
Maximum allowed SoC (SoC_{max})	90%

Source: (Kokam Module, 2017).

In the first simulation case, the ES-STATCOM will be connected to an equivalent ac system, as illustrated in Figure 23. The controlled voltage source used to represent the ac system, shown in Figure 23(b), receives the peak value of the voltage $\hat{V}_{s,k}$, obtained by multiplying the gain k_{V_s}, equal to the phase voltage peak value 7.97 kV, by the machine's excitation flux or magnetic flux Φ, considered to be 1. This operation constitutes a simplified representation of the electromotive force generated by the generation system. Additionally, the input frequency for the controlled voltage source f_s is defined by the block diagram at the bottom of Figure 23(b), which represents the swing equation of the generator system. The active power $P_{s,pu}$ is calculated using the voltages and currents measured at the connection point of the controlled voltage source with the grid. Once normalized, the calculated active power is compared with the normalized mechanical power $P_{mec,pu}$. The resulting error is directly multiplied by the system inertia J or $\left(\frac{1}{2H}\right)$, and passed through an integrator, given that the system damping B was neglected for simplicity in the present study. Accordingly, the inertia, the gains $k_{P_{mec}}$ and k_{Hz} were set to 0.17 pu, 2.5 pu and 60Hz, respectively.

For Cases B and C, the equivalent model of the ac system will also be used to represent the generator system dynamics; however, the gain $k_{\hat{V}_s}$ will be adjusted due to the different voltage level at the location where the controlled voltage source will be connected. Nevertheless, for all three simulation cases, the main parameters of the ES-STATCOM, the controller gains implemented in the converter's control structure, and the technical specifications of the battery modules used in the BESS adopted for the converter are presented in Tables 7, 8 and 9, respectively. Additionally, assuming a nominal voltage of 1.667kV for each SM, and based on the parameters in Table 9, the number of series-connected battery packs N_s was determined to be 28, the number of parallel strings N_p was set to 6, and the number of SM per arm was defined as 18. It should be noted that the battery racks are composed of ($N_s N_p$) battery packs, with only one rack connected to

Figure 23 – Schematic diagram of the ac system model.



Caption: (a) ac system equivalent model; (b) Grid control strategy.

Source: Prepared by the author (2025).

each SM in the distributed single-stage configuration.

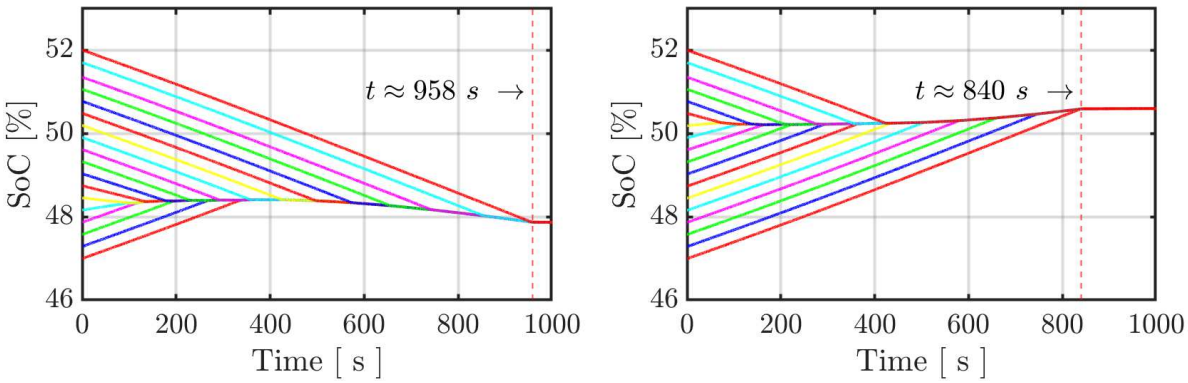
4.1 CASE A: SoC BALANCING PROCESS

As previously stipulated, Case A presents the different approaches carried out with regard to the SoC balancing process. These approaches are divided into two: Case A.1 and Case A.2, in which in the first one the balancing is performed exclusively using the instantaneous active and reactive powers. The second, however, is a refinement of the first approach, in which the balancing is performed only by compensating active power, using global SoC control to make the SoC values converge around a previously established reference value. Additionally, for this simulation case, it was considered that the 18 initial SoC values of each arm of the ES-STATCOM would be arranged within a range from 47% to 52%, evenly spaced from each other.

4.1.1 Case A.1: SoC balancing only with active power

The SoC balancing process using only the active power reference will be presented in this subsection. In this approach, the reference for the reactive power was kept at zero, thus ensuring that the ES-STATCOM only synthesizes active current at its terminals, allowing energy exchange between the converter and the ac system. Figure 24 illustrates the SoC dynamics in the upper arm of phase "a" during the balancing process. It can be observed that during the supply of active power (Figure 24(a)), that is, when the current at the ES-STATCOM terminals flows out towards the grid and discharging the batteries, the SoC converge around their average value at approximately instant $t \approx 958$s, reaching a value of 47.9%. On the other hand, during the absorption of active power (Figure 24(b)), that is, when the output current flows into the converter and charging the batteries, the SoC converge around $t \approx 840$s, stabilizing at a value of 50.6%. This difference in balancing time between both situations is due to the loss of capacity at nominal discharge current, which for the battery model used is approximately 20%.

Figure 24 – SoC balancing of the battery racks connected to the phase "a" upper arm of the ES-STATCOM using only active power.



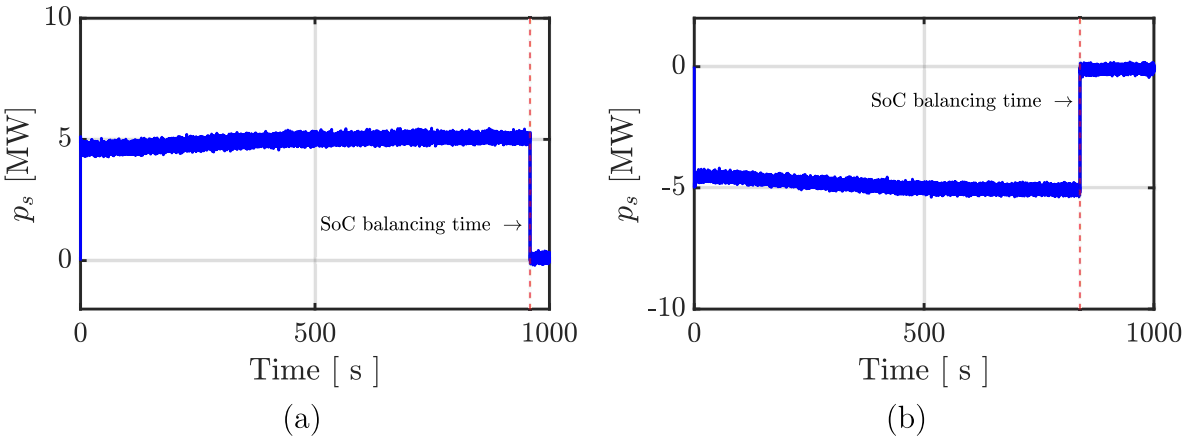
Caption: (a) ES-STATCOM supplying active power; (b) ES-STATCOM absorbing active power.

Source: Prepared by the author (2025).

Figure 25 denotes the instantaneous active power at the terminals of the ES-STATCOM for the SoC balancing through the batteries discharging and charging process. Active power references of +5MW and −5MW were adopted, respectively, for the SoC balancing through the discharge and charge of the batteries. It can be observed that the ES-STATCOM operates only during the time period necessary to achieve SoC balancing. It is also noticeable that during the first 400s, the active power does not remain around the reference. This can be attributed to the characteristics of the algorithm used for SoC balancing, since, due to the maximum modulation index limit adopted, there are always some SM that, while the batteries are discharging, temporarily operate in charging mode,

and while the batteries are charging, temporarily operate in discharging mode, until they converge to the average SoC value. At the end of the SoC balancing process, the reference of the active power goes to zero.

Figure 25 – Instantaneous active power at the ES-STATCOM ac terminals for Case A.1.



Caption: (a) SoC balancing process by discharging the batteries; (b) SoC balancing process by charging the batteries.

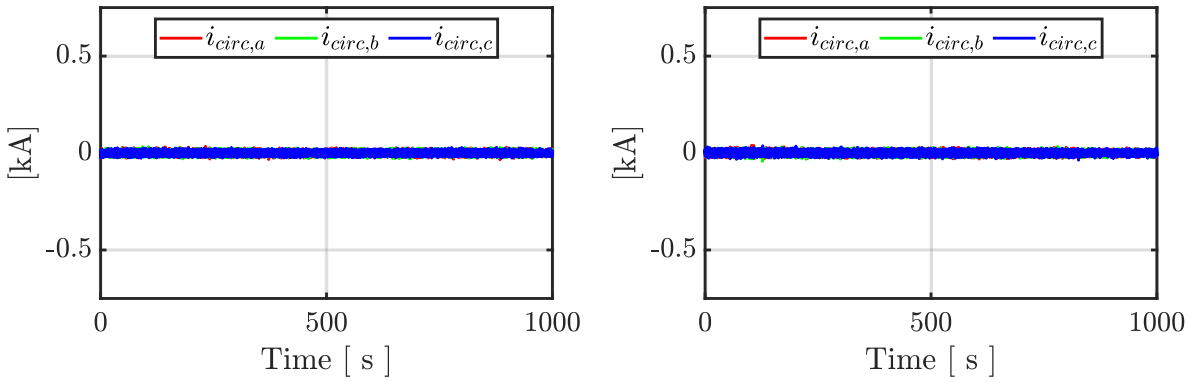
Source: Prepared by the author (2025).

As presented in the previous chapter, the control strategy for suppressing circulating currents through the arms of the ES-STATCOM is essential to ensure that the internal currents are compensated as effectively as possible. Although the adopted strategy represents a relatively simple approach, it proved to be sufficient to fulfill its intended purpose. Figure 26 illustrates the circulating currents in the three legs of the ES-STATCOM, where it can be clearly observed that, under both simulated scenarios, the internal currents are fully compensated.

In Figure 27, the three-phase currents synthesized by the ES-STATCOM for both simulated conditions are shown. It is observed that both during discharging and charging processes, the output currents have balanced characteristics with an RMS value of 353.55A. At $t = 200$s, in Figure 27(a), the currents present an average Total Harmonic Distortion (THD) of 1.48%, while in Figure 27(b) they present a value of 1.40%. As the SoC becomes more balanced, these THD values decrease, being 1.39% and 1.33%, respectively, in the last cycles of the currents before the end of their synthesis by the ES-STATCOM. These harmonic distortion values are due to the switching patterns that occur within the converter's SM.

The voltages at the terminals of the ES-STATCOM during the two simulated situations using only active power for Case A.1 are shown in Figure 28. It can be observed that in both simulated situations the terminal phase voltages remain balanced, assuming RMS values of 5.62kV, but they exhibit slight noise due to the internal switching of the

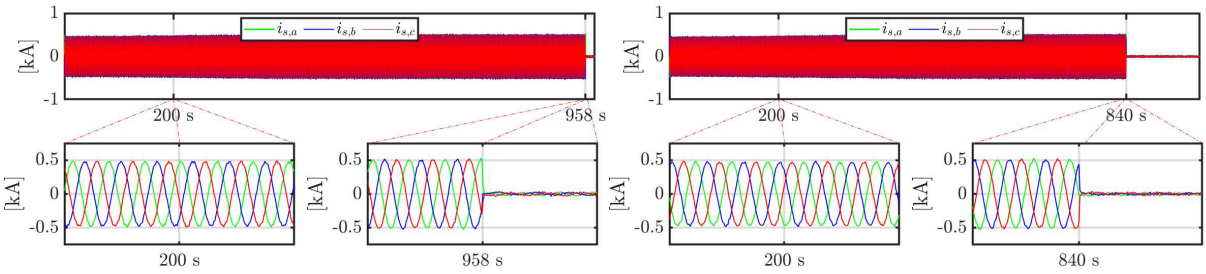
Figure 26 – Circulating currents through the ES-STATCOM arms using only active power for Case A.1.



Caption: (a) ES-STATCOM supplying active power; (b) ES-STATCOM absorbing active power.

Source: Prepared by the author (2025).

Figure 27 – Output currents synthesized by the ES-STATCOM using only active power for Case A.1.



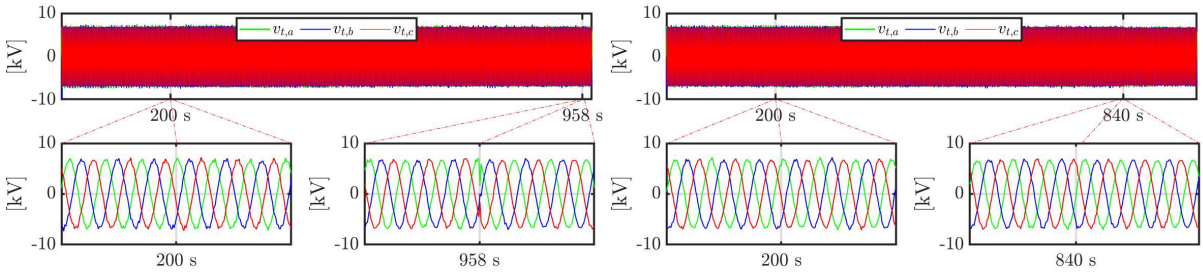
Caption: (a) ES-STATCOM supplying active power ; (b) ES-STATCOM absorbing active power.

Source: Prepared by the author (2025).

converter. At $t = 200$s, the average THD values are 3.03% and 2.99%, respectively, for the battery discharging and charging situations. At the SoC balancing instants, the harmonic distortions reach values of 2.44% and 2.35% in each situation.

Figure 29 illustrates the voltages of the battery racks connected to each SM in the upper arm of phase "a". It can be observed that in both balancing situations these voltages start with different values. As each battery rack reaches the convergence of its respective SoC value with the average SoC in the arm, its respective voltage also becomes equalized with the other already equalized voltages, assuming an average value equivalent to the nominal voltage specified for each SM, with an average value of 1.667kV. Note that the SoC balancing process is completed when the last voltage of sub-module N

Figure 28 – Voltages at the terminals of the ES-STATCOM using only active power for Case A.1.



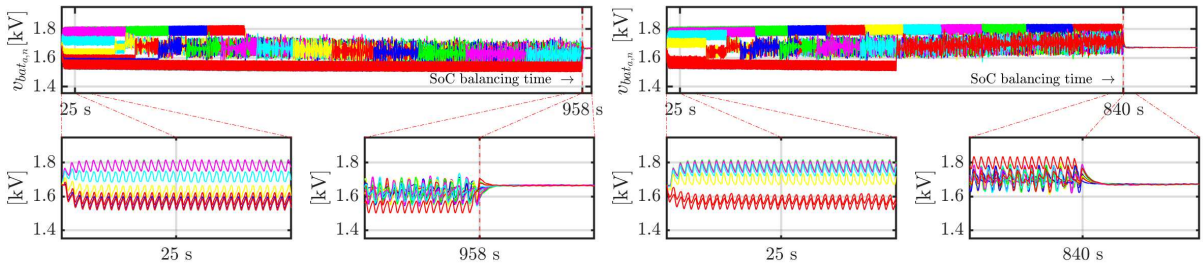
(a) (b)

Caption: (a) ES-STATCOM supplying active power; (b) ES-STATCOM absorbing active power.

Source: Prepared by the author (2025).

converges to the average value, becoming equalized with the other voltages. And once the ES-STATCOM has zero active power at its terminals, the already balanced SoC values remain constant at 47.9% and 50.6%, and the already equalized battery racks voltages remain constant at 1.667kV.

Figure 29 – Voltages of the battery racks in the phase "a" upper arm of the ES-STATCOM using only active power for Case A.1.



(a) (b)

Caption: (a) ES-STATCOM supplying active power; (b) ES-STATCOM absorbing active power.

Source: Prepared by the author (2025).

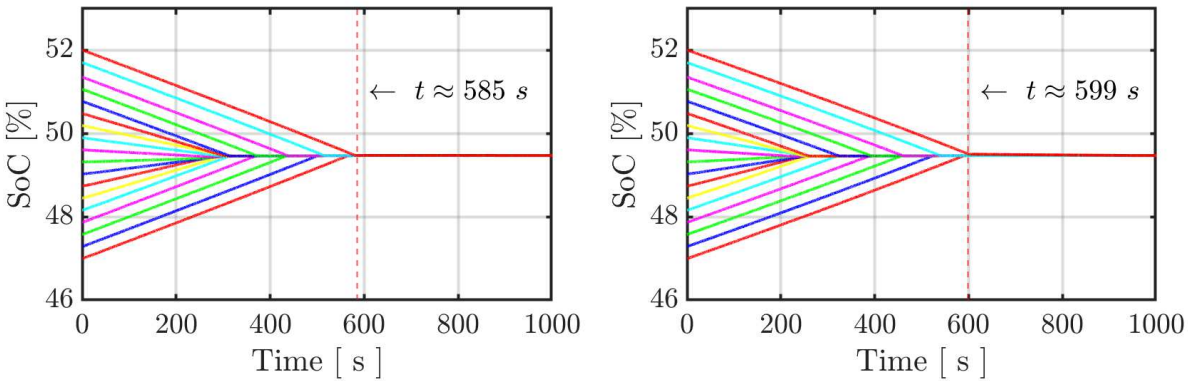
4.1.2 Case A.1: SoC balancing only with reactive power

In this subsection, the SoC balancing process using only the reactive power reference is presented. Under this condition, the active power is kept at zero, thus ensuring that the ES-STATCOM synthesizes only reactive current at its terminals. Since there is no active power flowing between the converter and the ac system, the average value of the SoC in each arm undergoes small variations due to converter losses, which can be neglected, remaining practically constant over time. Therefore, the balancing algorithm causes the

SoC values to converge to the average value in a shorter time, as currents flow through the arms of the ES-STATCOM, allowing it to supply reactive current at its terminals.

The existence of currents flowing through the converter arms enables energy exchange among the SM within the arms, causing the more charged modules to transfer energy to the less charged ones until balance is achieved. Figure 30 illustrates the SoC dynamics in the upper arm of phase "a" during the balancing process. It can be observed that during the supply of reactive power to the system, the SoC converge around their average value at approximately $t \approx 585$s, reaching a value of 49.5%. On the other hand, during the absorption of reactive power, the SoC converge around $t \approx 599$s, stabilizing at a value of 49.5%. This difference in balancing time between both situations is due to the losses associated with the arm and interface filters, as well as the reduction in capacity at the nominal discharge current of each battery pack.

Figure 30 – SoC balancing of the battery racks connected to the phase "a" upper arm of the ES-STATCOM using only reactive power.



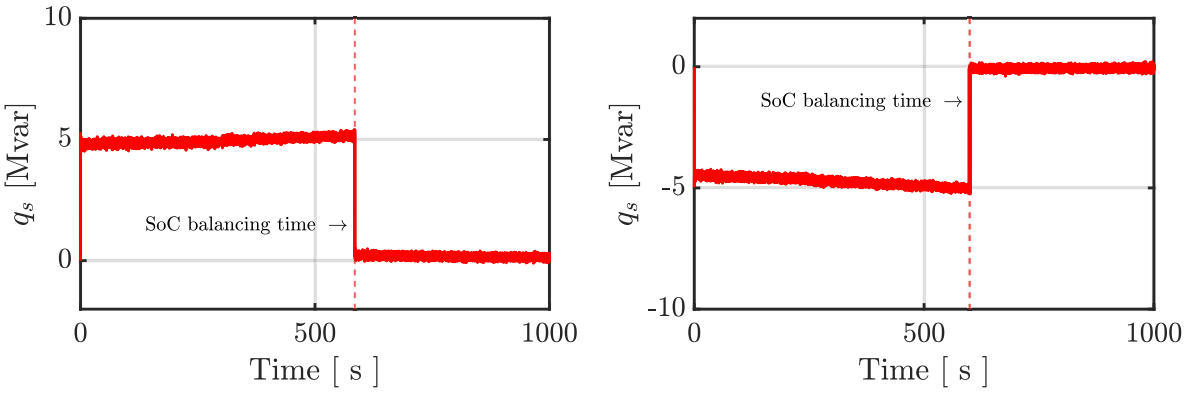
Caption: (a) ES-STATCOM supplying reactive power; (b) ES-STATCOM absorbing reactive power.

Source: Prepared by the author (2025).

Figure 31 shows the instantaneous reactive power at the terminals of the ES-STATCOM during the processes of supplying and absorbing reactive currents in the grid. The predefined reactive power references were set to +5Mvar and −5Mvar, respectively, until the SoC values were balanced, at which point the reference was set to zero upon convergence. Additionally, it can be observed that the reactive power takes around 400s to reach the reference, similar to the situation presented in the previous subsection. This can be attributed to the inductors that form the arm circuits and interface filters, with a more significant effect when the reactive current flows from the grid to the converter, due to the different dynamics during the charging and discharging processes of the battery racks.

Similarly to the operating conditions of the ES-STATCOM presented in the previous subsection, the circulating currents through the converter arms were completely

Figure 31 – Instantaneous reactive power at the ES-STATCOM ac terminals for Case A.1.

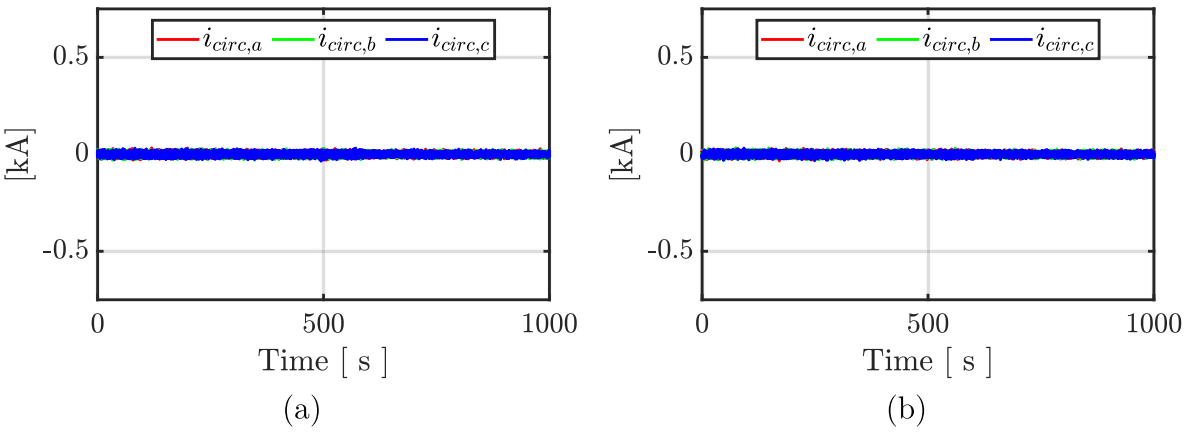


Caption: (a) ES-STATCOM supplying reactive power ; (b) ES-STATCOM absorbing reactive power.

Source: Prepared by the author (2025).

compensated solely by employing the CCSC strategy. Figure 32 illustrates the behavior of the circulating currents in each phase of the converter during the supply and absorption of reactive power at the ac terminals in the SoC balancing process.

Figure 32 – Circulating currents through the ES-STATCOM arms using only reactive power for Case A.1.



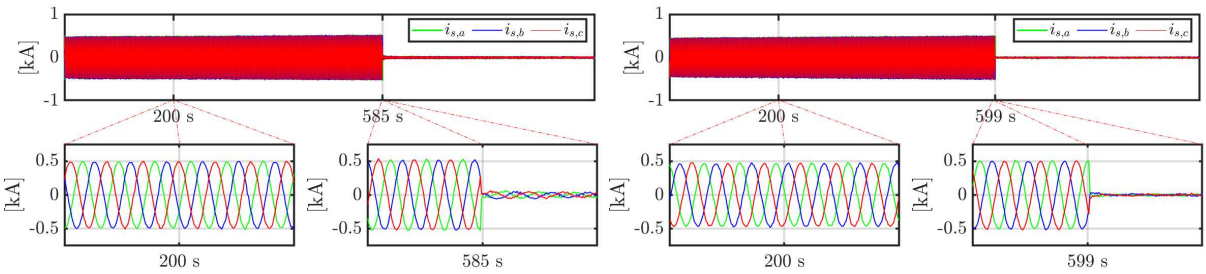
Caption: (a) ES-STATCOM supplying reactive power; (b) ES-STATCOM absorbing reactive power.

Source: Prepared by the author (2025).

The three-phase currents synthesized by the ES-STATCOM are shown in Figure 33. It can be observed that under both conditions, the currents remain balanced with an RMS value of 353.55A. Figure 33(a) shows the dynamics of the currents during the SoC balancing process while supplying reactive power to the grid, presenting an average THD of 1.31% at $t = 200$s and 1.28% just before the balancing time at $t \approx 585$s. Figure 33(b)

shows the currents under the condition of reactive power absorption to perform the SoC balancing, where average THD values of 1.36% and 1.29% were obtained at $t = 200$s and just before $t \approx 599$s, respectively. It should be noted that, in this situation as well, a decrease in THD occurred as the SoC values became balanced, which is attributed to the reduction in switching operations within the SM during the SoC balancing process.

Figure 33 – Output currents synthesized by the ES-STATCOM using only reactive power for Case A.1.



(a) (b)

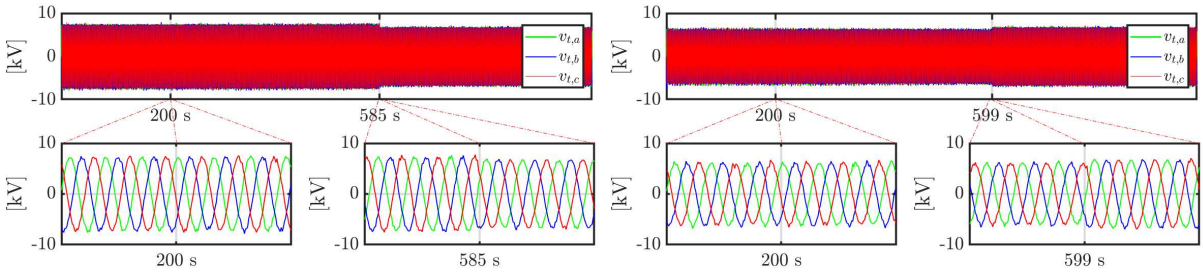
Caption: (a) ES-STATCOM supplying reactive power; (b) ES-STATCOM absorbing reactive power.

Source: Prepared by the author (2025).

Figure 34 presents the voltages at the terminals of the ES-STATCOM under the two simulated conditions for Case A.1 using only reactive power. It is possible to observe that, in both conditions, the three-phase voltages are balanced, with RMS values varying due to the reactive compensation at the converter terminals. During the supply of reactive power, the voltages have an RMS value of 5.901kV with an average THD of 2.35% at $t = 200$s. When the ES-STATCOM is absorbing reactive power from the grid, the voltages present an RMS value of 5.34kV with an average THD of 2.43% at $t = 200$s. Once the SoC balancing is completed, the converter ceases to operate, reducing the reactive power at its terminals to zero, causing the voltages to return to an RMS value of 5.62kV with an average THD of approximately 1.91% in both conditions.

The voltages of each battery rack connected to each SM in the upper arm of phase "a" of the ES-STATCOM are illustrated in Figure 35. It should be noted that, in both simulated conditions, the initial voltage values are different from each other; as the SoC balancing process occurs, these voltages gradually equalize around the nominal average value of each SM, which is 1.667kV. Thus, once the voltages are fully equalized, it indicates that the SoC values are balanced around the average value of the arm, allowing the ES-STATCOM to cease operation, with the SoC and the battery rack voltages remaining constant at approximately 49.5% and 1.667kV, respectively.

Figure 34 – Voltages at the terminals of the ES-STATCOM using only reactive power for Case A.1.

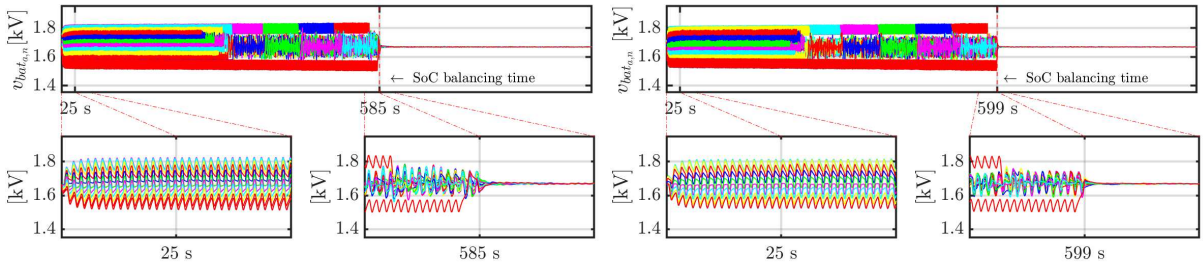


(a) (b)

Caption: (a) ES-STATCOM supplying reactive power; (b) ES-STATCOM absorbing reactive power.

Source: Prepared by the author (2025).

Figure 35 – Voltages of the battery racks in the phase "a" upper arm of the ES-STATCOM using only reactive power for Case A.1.



(a) (b)

Caption: (a) ES-STATCOM supplying reactive power; (b) ES-STATCOM absorbing reactive power.

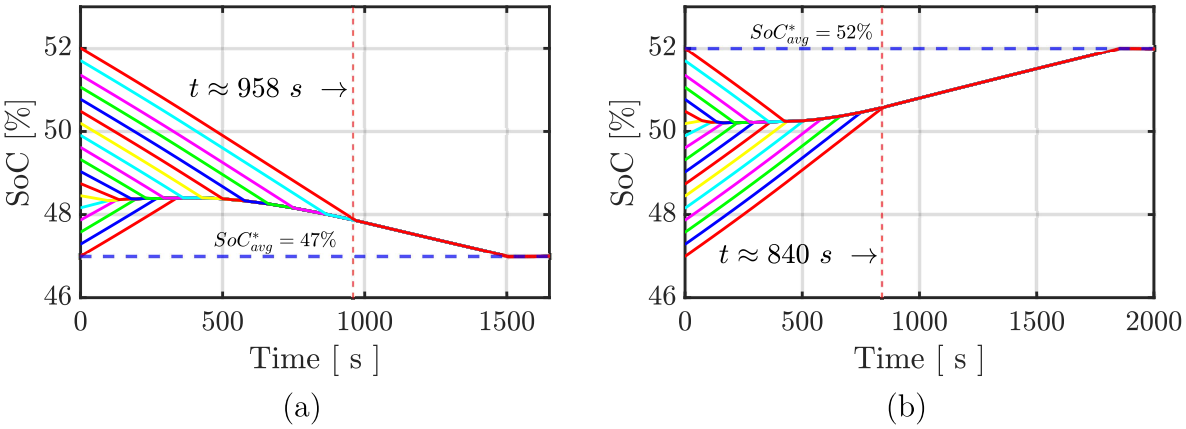
Source: Prepared by the author (2025).

4.1.3 **Case A.2**

In this case, an improved approach to Case A.1 using only active power will be presented. This means that the SoC balancing process will be carried out through a global SoC control loop, which takes as inputs the measured SoC values of each SM and a reference value SoC^*_{avg}. Consequently, the same control loop will output the active three-phase currents, which must be transformed to the SRF, so that the q-axis component can be used as the reference for the current control loop of the ES-STATCOM, leaving the SoC values already balanced and equal to the previously set SoC reference. The use of the q-axis component is due to the design of the PLL; therefore, the quadrature-axis current is associated with active power, while the direct-axis current is associated with reactive power.

Figure 36 shows the behavior of the SoC of the battery racks connected to the SM

Figure 36 – SoC balancing of the battery racks connected to the phase "a" upper arm of the ES-STATCOM during Case A.2.



Caption: (a) ES-STATCOM supplying active power; (b) ES-STATCOM absorbing active power.

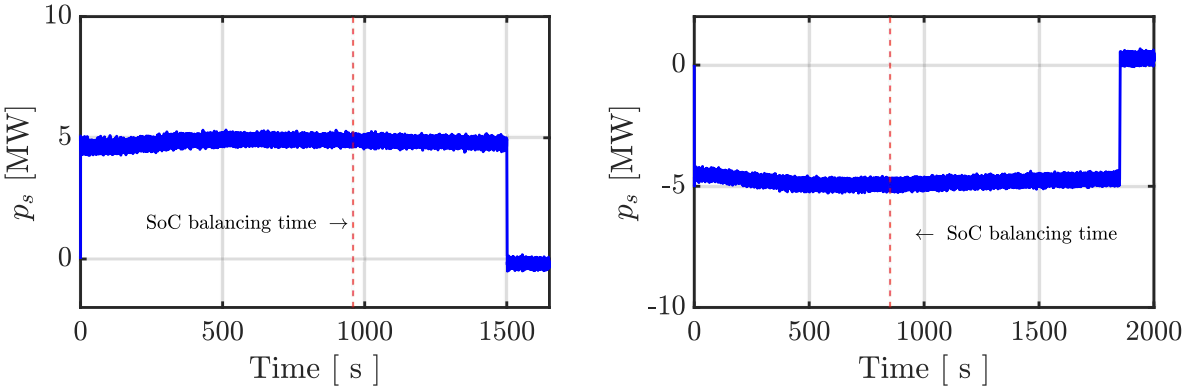
Source: Prepared by the author (2025).

in the upper arm of phase "a" of the ES-STATCOM during the SoC balancing process under two distinct simulated situations. The first situation sets a reference SoC of 47%, as illustrated in Figure 36(a). It can be observed that the SoC values are balanced at approximately $t \approx 958$s, the same time as seen in Case A.1; however, the battery racks continue to discharge until they reach the reference value at $t = 1500$s. The second situation illustrated in Figure 36(b), occurs when the SoC^*_{avg} is set at 52%. Again, the SoC values are balanced at the same time as in Case A.1, at approximately $t \approx 840$s, but now the battery racks are charged until they reach the reference at $t = 1850$s. This difference in the time required for the SoC values to reach their respective reference values is due to the 20% loss of the nominal discharge current capacity of the battery model used. As a result, the average SoC tends to decrease and increase at different rates in each situation. That is, when the batteries are discharged, the average SoC decreases with a higher rate of change, making the balancing process longer, but the reference SoC^*_{avg} is reached in less time. Conversely, when the batteries are charged, the average SoC tends to increase at a lower rate of change, resulting in a shorter balancing time but requiring more time to reach the SoC^*_{avg} reference.

In Figure 37, it is possible to observe the instantaneous active power at the terminals of the ES-STATCOM during the battery discharging and charging situations, respectively. In the first situation, approximately +4.9MW was required to bring the SoC values to around 47%, and once this value was reached, the ES-STATCOM was turned off. In the second situation, in which the battery racks are charged, approximately −4.9MW was needed to bring the SoC values to around 52%.

Similarly to the previous sub-case, a control loop aimed at suppressing the internal

Figure 37 – Instantaneous active power at the ES-STATCOM ac terminals during Case A.2.

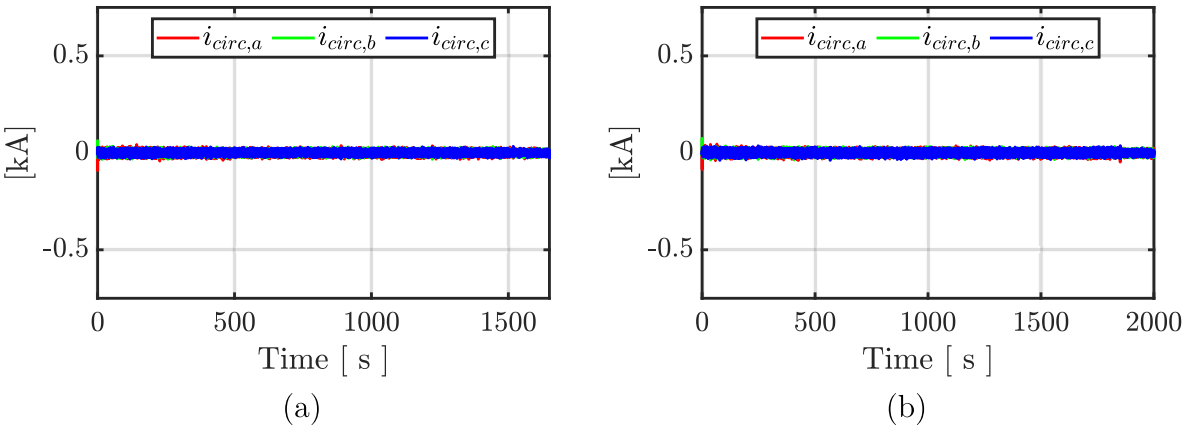


Caption: (a) SoC balancing process by discharging the batteries; (b) SoC balancing process by charging the batteries.

Source: Prepared by the author (2025).

currents of the ES-STATCOM is employed. In Figure 38, it is possible to observe the circulating currents through the arms of the ES-STATCOM; it can be seen that they are completely suppressed in both simulated situations, noting that these currents lack a continuous component due to the open circuit in the dc bus.

Figure 38 – Circulating currents through the ES-STATCOM arms using only active power during Case A.1.



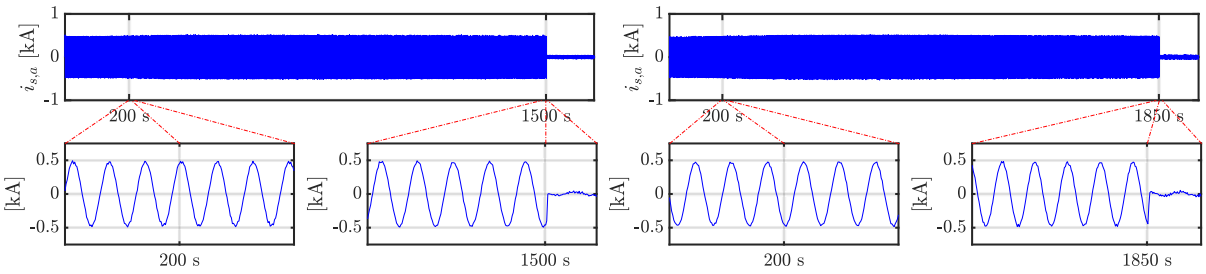
Caption: (a) ES-STATCOM supplying active power ; (b) ES-STATCOM absorbing active power.

Source: Prepared by the author (2025).

Figure 39 illustrates phase "a" of the output current synthesized by the ES-STATCOM in the two simulated situations during Case A.2. As seen in Case A.1, the three-phase currents and voltages at the converter terminals exhibit balanced characteristics; thus,

for simplicity and to facilitate graphical analysis, only phase "a" of these quantities was plotted for this case. In Figure 39(a), the dynamics of phase "a" of the current during the battery discharging process can be observed, showing an average THD across the three phases of 1.85% at $t = 200$s and 1.02% just before the ES-STATCOM is turned off at $t = 1500$s. Figure 39(b) shows the same phase of the output current during the battery charging process, where average THD values across the three phases of 1.78% and 0.99% were obtained at $t = 200$s and just before $t = 1850$s, respectively. Additionally, in both simulated situations, the currents presented an RMS value of 353.55A.

Figure 39 – Phase "a" output current synthesized by the ES-STATCOM during Case A.2.



(a) (b)

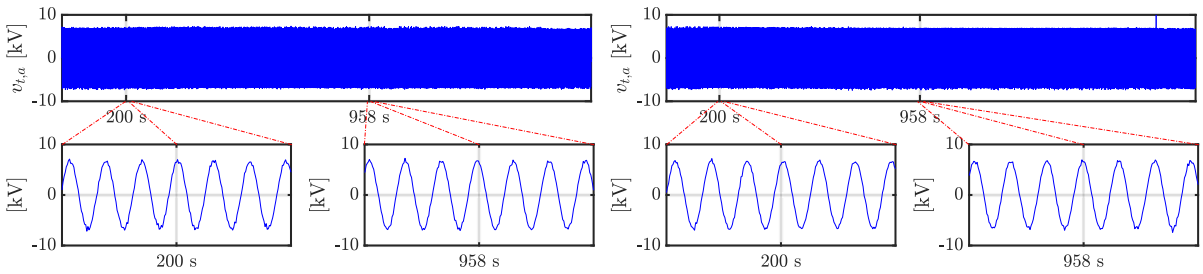
Caption: (a) ES-STATCOM supplying active power ; (b) ES-STATCOM absorbing active power.

Source: Prepared by the author (2025).

As previously explained, Figure 40 shows the behavior of phase "a" voltage at the terminals of the ES-STATCOM during both simulated situations. Both during the discharging and charging processes of the battery racks, the three-phase voltages exhibit a balanced behavior similar to Case A.1, presenting an average THD across the three phases of 3.01% and 2.98% at $t = 200$s, then 2.42% and 2.40% at $t = 958$s. Note that as the SoC values become balanced, the harmonic distortion decreases due to the fact that the internal switching pattern of the SM becomes smoother.

Finally, the battery rack voltages in phase "a" of the upper arm of the ES-STATCOM during the two simulated situations are shown in Figure 41. It can be noted that in both situations, the SM start with different voltage values; as the SoC balancing process progresses, the voltages are gradually equalized. Once the SoC are balanced, the SM voltages become fully equalized, presenting an average value of 1.667kV. The SM voltages remain equalized, exhibiting a waveform very close to a triangular shape until the moments when the SoC values reach their respective reference values SoC^{*}_{avg}, subsequently remaining constant at the nominal SM voltage of 1.667kV.

Figure 40 – Phase "a" voltage at the terminals of the ES-STATCOM during Case A.2.

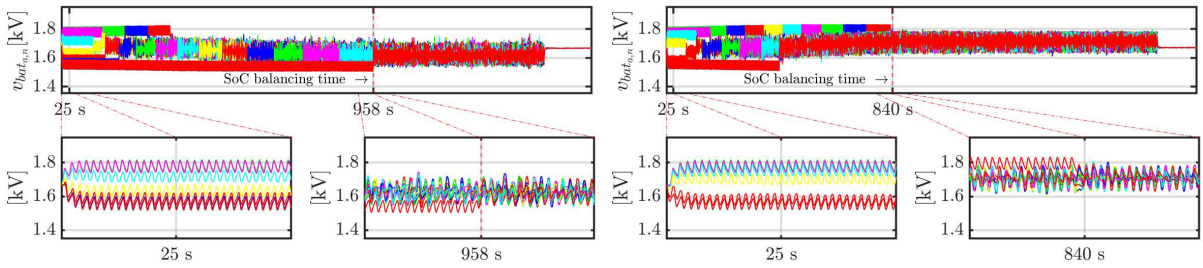


(a) (b)

Caption: (a) ES-STATCOM supplying active power ; (b) ES-STATCOM absorbing active power.

Source: Prepared by the author (2025).

Figure 41 – Voltages of the battery racks in the phase "a" upper arm of the ES-STATCOM during Case A.2.



(a) (b)

Caption: (a) ES-STATCOM supplying active power ; (b) ES-STATCOM absorbing active power.

Source: Prepared by the author (2025).

4.2 CHAPTER REMARKS

This chapter presented the simulations of the ES-STATCOM connected to a balanced ac system, focusing specifically on Case A, which addressed the SoC balancing process under different operating conditions. The simulation results demonstrated the effectiveness of the proposed balancing approaches using both active and reactive power control strategies, as well as an enhanced approach using active power for the SoC balancing process by a global SoC control.

In Case A.1, it was verified that SoC balancing can be successfully achieved through both active and reactive power compensation. When using only active power, the SoC values converged to a balanced state during both charging and discharging cycles, despite inherent asymmetries in balancing times due to battery capacity degradation at nominal discharge currents. Conversely, the use of reactive power for SoC balancing allowed for

effective internal energy redistribution among the converter's SM without the need for net active power exchange with the grid. This approach also resulted in slightly faster convergence times compared to the active power-only strategy.

Furthermore, the circulating current suppression strategy applied in all scenarios effectively minimized internal circulating currents within the converter, thereby ensuring stable operation and low harmonic distortion in the synthesized currents and voltages. The simulation results consistently showed that both current and voltage waveforms maintained balanced profiles with low THD throughout the SoC balancing processes.

Finally, Case A.2 introduced a refined global SoC control strategy utilizing only active power to enforce convergence of all SoC values towards a predefined SoC reference. The simulations demonstrated that this approach not only ensured balanced SoC values but also provided precise control over the final SoC levels. However, the required balancing duration was influenced by the discharging characteristics of the batteries used, that also influence de rate of change of the average value of the SoC in each arm, with longer times observed when charging the batteries.

Overall, the simulation results verified the effectiveness of the ES-STATCOM control architecture for SoC balancing under various power exchange scenarios, thus establishing a solid foundation for subsequent analyses related to frequency and voltage support functionalities, which will be addressed in the following chapter.

5 ANCILLARY SERVICES SIMULATION CASE

Once the balancing process of the SoC has been successfully completed, as thoroughly described in Chapter 4, the ES-STATCOM is ready to provide ancillary services to the ac system. These services are essential for enhancing system reliability, stability, and overall operational efficiency. Therefore, this chapter is dedicated to presenting and analyzing the simulation results related to two distinct ancillary services provided by the ES-STATCOM when connected to a modified IEEE-14 bus system, which have been modeled using PSCAD/EMTDC. The first scenario involves the response of the ES-STATCOM during the connection of a significantly large load, designated as Case B. The second scenario focuses on the behavior of the ES-STATCOM during a symmetrical fault in the ac system, referred to as Case C, which represents a severe and critical condition for system stability.

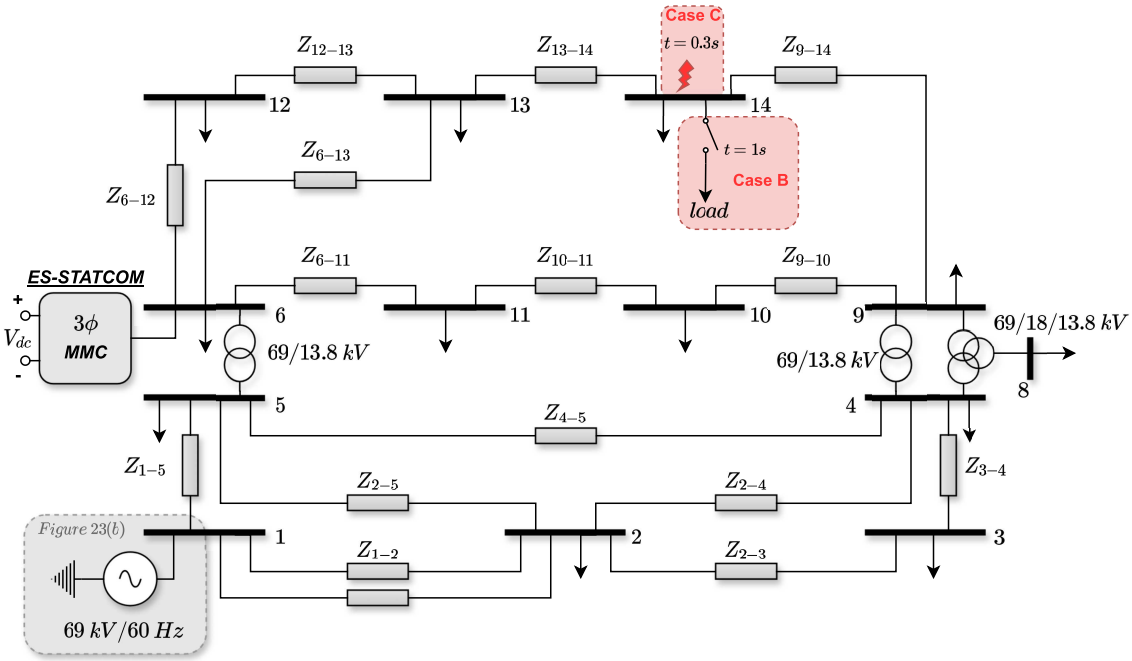
Figure 42 depicts the modified IEEE 14-bus system adopted for the simulation of these two cases. This benchmark system has been adapted to accommodate the ES-STATCOM at bus 6, where the local line-to-line voltage is 13.8kV. Additionally, the controlled voltage source, which serves as a representation of the generation system, is connected at bus 1 of the network. It is important to highlight that the only modification in the simulation parameters, when compared to those utilized in the previous chapter, pertains to the voltage level at which the controlled source, illustrated in Figure 23(b), is connected. In this chapter, the controlled source operates at 69kV line-to-line, needing an adjustment in the gain parameter $k_{\hat{V}_s}$, which is now set to 39.84kV. All other simulation parameters, including converter topology and control configurations, remain consistent with those adopted in Chapter 4. For completeness, the specific parameters of the transmission lines and the load characteristics at each bus are systematically presented in Tables 10 and 11, respectively.

Table 10 – Transmission line parameters.

Line	**R** (Ω)	**X** (Ω)	**Line**	**R** (Ω)	**X** (Ω)
1–2	6.15	18.78	6–11	1.20	2.52
1–5	17.14	70.79	6–12	1.56	3.25
2–3	14.91	62.83	6–13	1.68	3.31
2–4	18.44	55.96	7–8	0.022	2.24
2–5	18.07	55.19	7–9	0.014	1.40
3–4	21.27	54.28	9–10	0.40	1.07
4–5	4.24	13.36	9–14	5.32	11.33
4–7	0.66	66.37	10–11	5.73	13.41
4–9	1.76	176.53	12–13	2.80	2.54
5–6	0.80	80.00	13–14	2.17	4.42

Source: (DUARTE; ALMEIDA; BARBOSA, 2022).

Figure 42 – Modified IEEE 14-bus system.



Source: Adapted from Duarte, Almeida e Barbosa (2022).

Table 11 – System load parameters.

Bus	P (MW)	Q (Mvar)	Bus	P (MW)	Q (Mvar)
1	–	–	8	–	–
2	1.085	0.635	9	2.2125	1.245
3	4.710	0.950	10	0.450	0.290
4	2.390	–0.195	11	0.175	0.090
5	0.190	0.040	12	1.3725	0.360
6	0.084	0.05625	13	0.675	0.290
7	–	–	14	1.1175	0.375

Source: (DUARTE; ALMEIDA; BARBOSA, 2022).

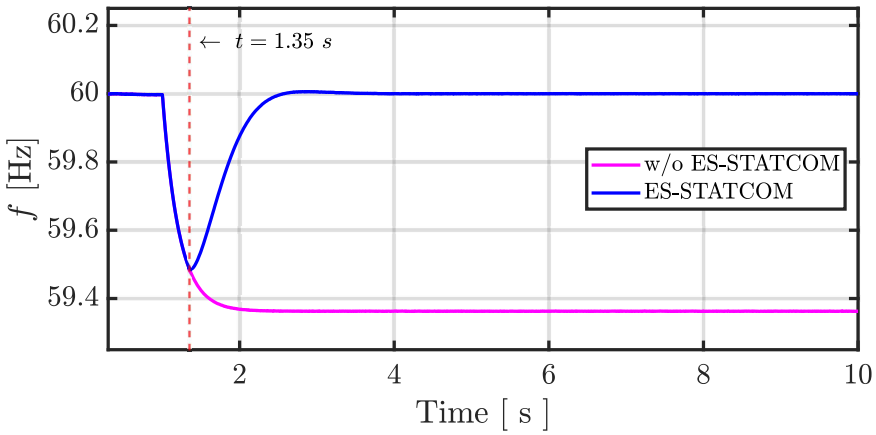
5.1 CASE B: FREQUENCY SUPPORT

For the first simulation case of ancillary service provision by the ES-STATCOM, the approach chosen was frequency disturbance mitigation in the ac system. To this end, a balanced load of 3.5MW was applied at bus 14 at $t = 1$ s. Once the frequency disturbance occurred, the ES-STATCOM started operating as soon as the system frequency f reached a minimum limit of 59.5Hz, initiating the injection of active power into the system and providing frequency support.

Figure 43 shows the dynamics of the electrical frequency f behavior during the frequency support simulation case. It is observed that before the connection of the large

load, the electrical frequency is at 60Hz. As soon as the load is connected at $t = 1$ s, the frequency starts to decrease. Once the minimum limit, defined as 59.5Hz, is reached at $t = 1.35$ s, the frequency support control activates the ES-STATCOM to start injecting active power into the electrical grid, causing the frequency to rise toward its nominal value. Note that in the absence of the ES-STATCOM, the system's electrical frequency would drop below 59.4Hz, a value that is undesirable for the operation of medium-voltage ac systems.

Figure 43 – Dynamic behavior of electrical grid frequency during the load disturbance.



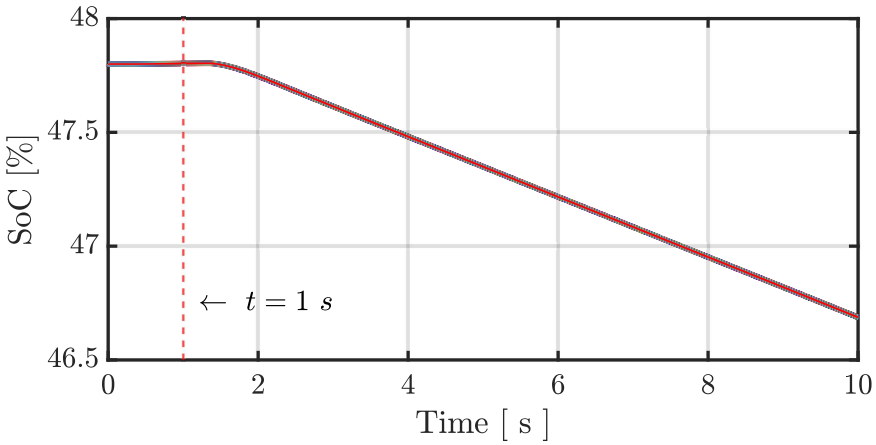
Source: Prepared by the author (2025).

It is important to emphasize that this behavior in the electrical frequency is only possible in this simulation, since in real situations an ES-STATCOM would not have sufficient energy to fully eliminate the frequency deviation. In other words, the converter would not be able to take control of the entire system; it would only support the primary frequency regulation, preventing the nadir from dropping too low and maintaining the frequency at an acceptable level below 60Hz during the first seconds of the disturbance. The electrical frequency would then be restored by other generation sources of the system through secondary frequency regulation.

Figure 44 illustrates the behavior of the already balanced SoC values of the battery rack connected to each SM of the upper arm of phase "a" of the ES-STATCOM during the frequency support process after the connection of a large load in the ac system. It can be observed that the SoC values remain constant at 47.88% during the initial moments after the load connection. When the load is connected at $t = 1$ s, the SoC values still remain constant until the moment when the electrical frequency reaches its minimum allowed value of 59.5Hz at $t = 1.35$ s. Once the ES-STATCOM starts operating by injecting active power into the grid, the batteries are discharged, causing the SoC values to decrease during the frequency support process.

The instantaneous active and reactive powers at the ac terminals of the ES-STATCOM during the frequency support process are shown in Figure 45. It is possible to notice

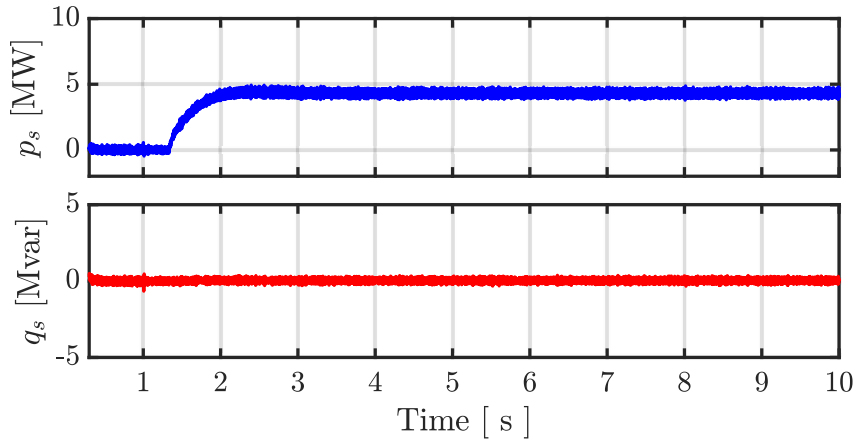
Figure 44 – SoC dynamics of the battery racks connected to the phase "a" upper arm of the ES-STATCOM during Case B.



Source: Prepared by the author (2025).

the moment when the large load is connected through slight peaks at $t = 1$ s in both the active and reactive powers dynamics behavior. While the instantaneous reactive power has an average value equal to zero throughout the entire frequency support process, the instantaneous active power starts to be injected into the grid at $t = 1.35$ s. Once the electrical frequency reaches the reference value of 60Hz, the active power at the AC terminals of the ES-STATCOM stabilizes at an approximately constant average value of 4.85MW.

Figure 45 – Instantaneous active and reactive power at the ES-STATCOM ac terminals during Case B.

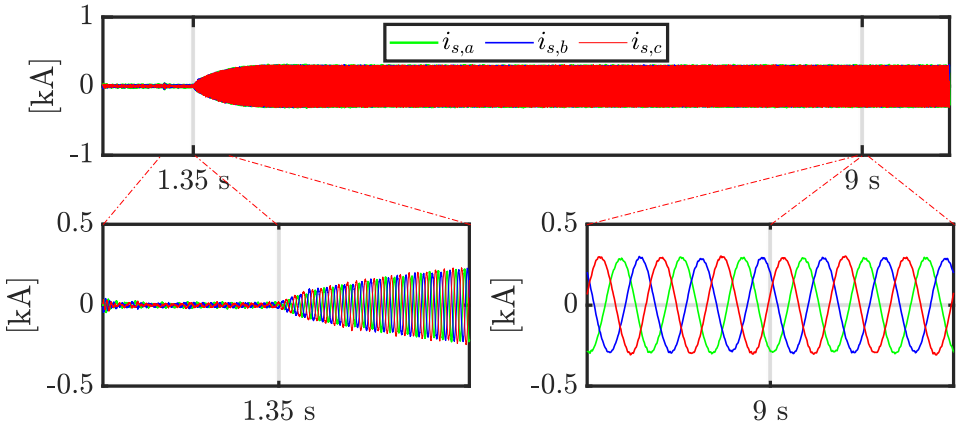


Source: Prepared by the author (2025).

In Figure 46, it is possible to observe the behavior of the three-phase currents synthesized by the ES-STATCOM during the electrical frequency support process in the ac system. It can be seen that the ES-STATCOM starts synthesizing currents only from the instant $t = 1.35$ s, since at that moment the frequency support control is activated to

proceed with the compensation of the electrical frequency through the injection of active power into the grid. The three-phase currents exhibit a balanced behavior throughout the simulated process, with an average THD of the three phases equal to 0.93% at $t = 9$ s, and assuming an RMS value of approximately 192A in each phase.

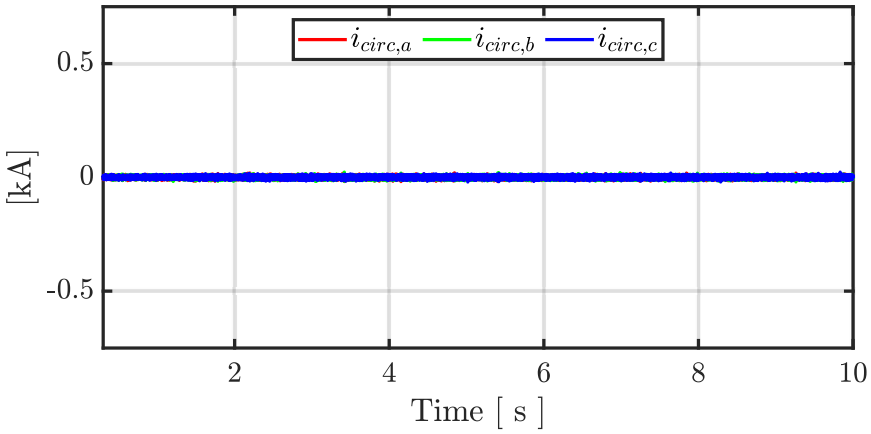
Figure 46 – Output currents synthesized by the ES-STATCOM during the grid frequency support.



Source: Prepared by the author (2025).

Figure 47 shows the circulating currents through the arms of the ES-STATCOM during the frequency support process. As in Case A, the CCSC control loop was also used in this case to suppress the converter's internal currents. It can be seen that the currents flowing through the three arms of the ES-STATCOM are fully compensated, assuming a mean value of zero in all three phases, validating the good performance of the adopted control strategy.

Figure 47 – Circulating currents through the ES-STATCOM arms during Case B.

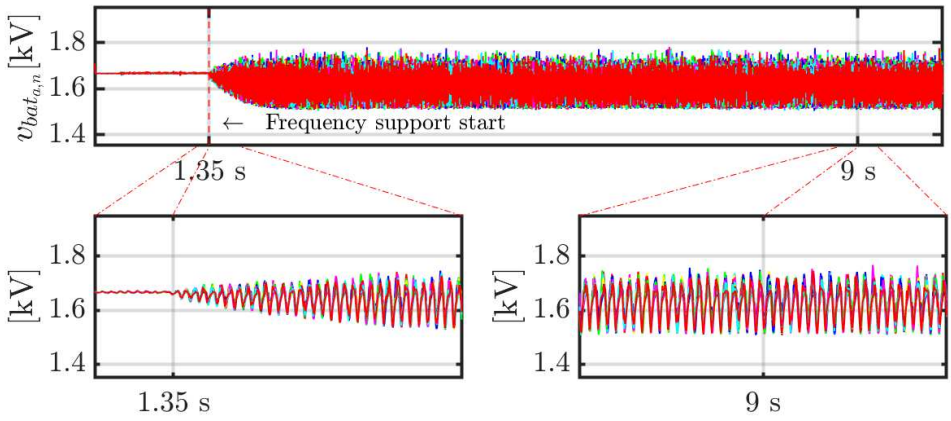


Source: Prepared by the author (2025).

The dynamic behavior of the battery rack voltages connected to phase "a" in the upper arm of the ES-STATCOM during the frequency support process is shown in

Figure 48. It can be observed that the voltages start off equalized with constant values of 1.667kV. From the moment the frequency support begins, at $t = 1.35$ s, the batteries start operating, causing their respective voltages to exhibit triangular waveform with an average value of 1.667kV. This oscillatory behavior is a direct consequence of the modulation and power exchange dynamics between the ES-STATCOM and the grid during the active power injection. Despite the variations, the voltages remain centered around their nominal value throughout the entire frequency support process, ensuring the proper and balanced operation of the system.

Figure 48 – Voltages of the battery racks in the upper arm of phase "a" of the ES-STATCOM during Case B.



Source: Prepared by the author (2025).

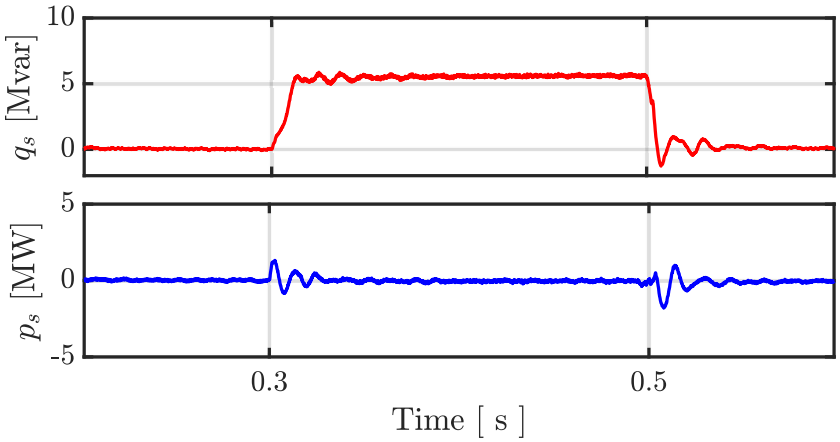
5.2 CASE C: VOLTAGE SUPPORT

The last simulation case is Case C, which will be presented in this section. In this final case, an analysis is carried out of the response of the modeled ES-STATCOM to a voltage disturbance caused by a symmetrical fault, applied at bus number 14 during the time interval of 0.3 s $\leq t \leq$ 0.5 s. The ES-STATCOM remains floating in the IEEE 14-bus system until the symmetrical fault occurs, triggering the control of the positive sequence of the d-axis component of the voltage measured at the PCC, and injecting reactive power into the grid so that the converter can provide voltage support at its point of connection.

Figure 49 illustrates the behavior of the instantaneous reactive and active powers at the ac terminals of the ES-STATCOM during the occurrence of the three-phase-to-ground fault in the ac system. According to the parameters adopted for the modeling of the ES-STATCOM, the maximum reactive power it is capable of injecting was delivered to the grid, being equal to 5.65Mvar during the fault duration. Note that the converter is able to inject the reactive power without exhibiting significant peak values. The active power at the terminals only undergoes small perturbations at the moments of the beginning and end of the fault occurrence, maintaining a zero mean value throughout the simulation.

Additionally, it is remarkable that since there is only reactive power at the terminals of the ES-STATCOM, the SoC values remain practically constant throughout the fault occurrence, as there is no active power flow between the converter and the electrical grid.

Figure 49 – Instantaneous reactive and active power at the ES-STATCOM ac terminals during Case C.



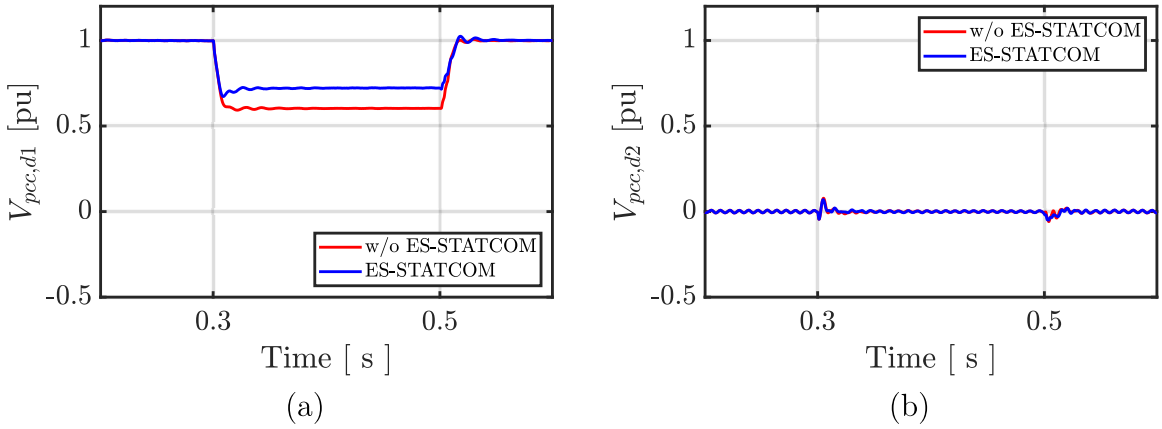
Source: Prepared by the author (2025).

Figure 50 shows the dynamic behavior of the *d*-axis component of the voltage at the PCC in its positive and negative sequences during the fault. The nominal line voltage at the point where the ES-STATCOM was connected was adopted as the voltage base, as illustrated in Figure 42. In Figure 50(a), it can be observed that the positive sequence of the *d*-axis voltage at the PCC is at 1 *pu* during the pre-fault and post-fault periods; during the fault, the voltage drops to 0.73 *pu*. In the case of the fault occurring without the ES-STATCOM, the voltage at bus 6 drops to 0.6 *pu*. Finally, Figure 50(b) shows the behavior of the negative sequence of the voltage at the PCC. It can be seen that it remains at zero both with and without the ES-STATCOM.

The dynamic behavior of the *d*-axis component of the currents synthesized by the ES-STATCOM in its positive and negative sequences during the fault is shown in Figure 51. It is evident that, in the case where the converter is not operating, its output currents will be null. Figure 51(a) shows the positive sequence of the *d*-axis component during the fault; it assumes a value of 0.5kA, without exhibiting significant peak values. This positive sequence reactive current injected by the ES-STATCOM into the grid provides voltage support. The negative sequence of the current, shown in Figure 51(b), undergoes small perturbations at the initial and final moments of the fault, maintaining a zero mean value throughout the simulation.

Figure 52 illustrates the behavior of the three-phase voltages at the PCC during the fault event. It can be observed that the voltages exhibit a balanced behavior during the pre-fault, fault, and post-fault periods. The dynamics of the voltages at the PCC are shown both with and without the operation of the ES-STATCOM. In Figure 52(a),

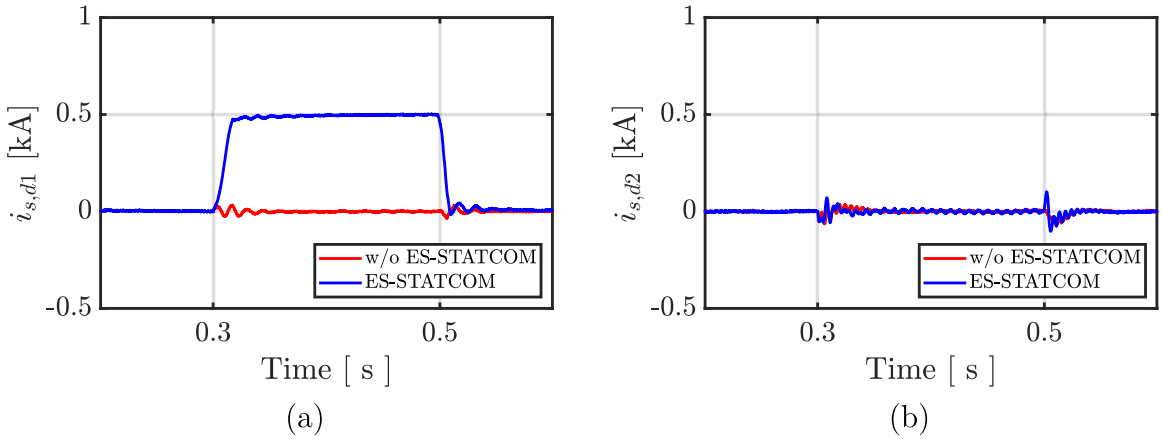
Figure 50 – Dynamic behavior of the d-axis component of the PCC voltage during Case C.



Caption: (a) Positive sequence component; (b) Negative sequence component.

Source: Prepared by the author (2025).

Figure 51 – Dynamic behavior of the d-axis component of the currents synthesized by the ES-STATCOM during Case C.



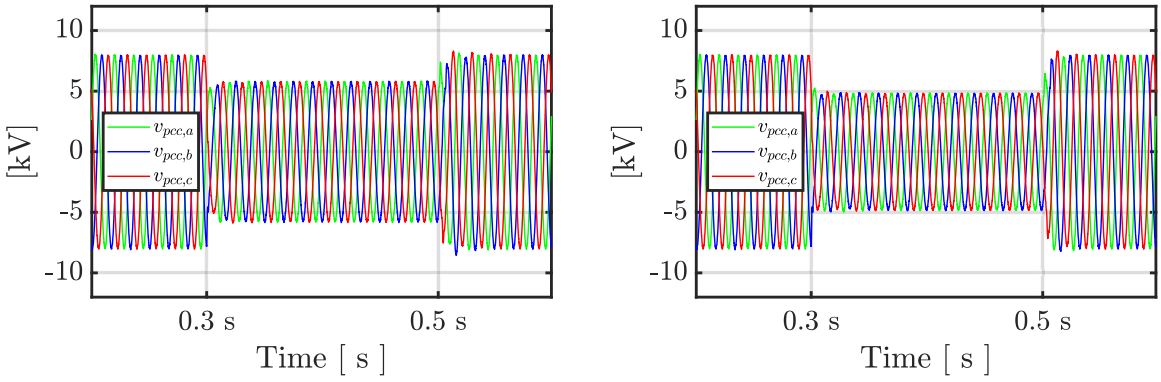
Caption: (a) Positive sequence component; (b) Negative sequence component.

Source: Prepared by the author (2025).

the converter operates during the fault, providing voltage support; during the fault, the average THD across the three phases is 1.27% and the RMS voltage value is 4.11kV. Figure 52(b) shows the behavior of the voltages at the PCC without the operation of the ES-STATCOM during the fault; during its duration, the average THD of the three-phase voltage is 1.21%, with an RMS value of 3.38kV.

The three-phase currents synthesized by the ES-STATCOM during the fault are illustrated in Figure 53; these currents are measured at the output of the converter. In Figure 53(a), it is possible to observe the current synthesis performed by the ES-STATCOM during the fault duration, that is, the injection of reactive power for the purpose of compensating the voltage at the converter's point of connection with the ac system. Note

Figure 52 – Voltages at the PCC during Case C.

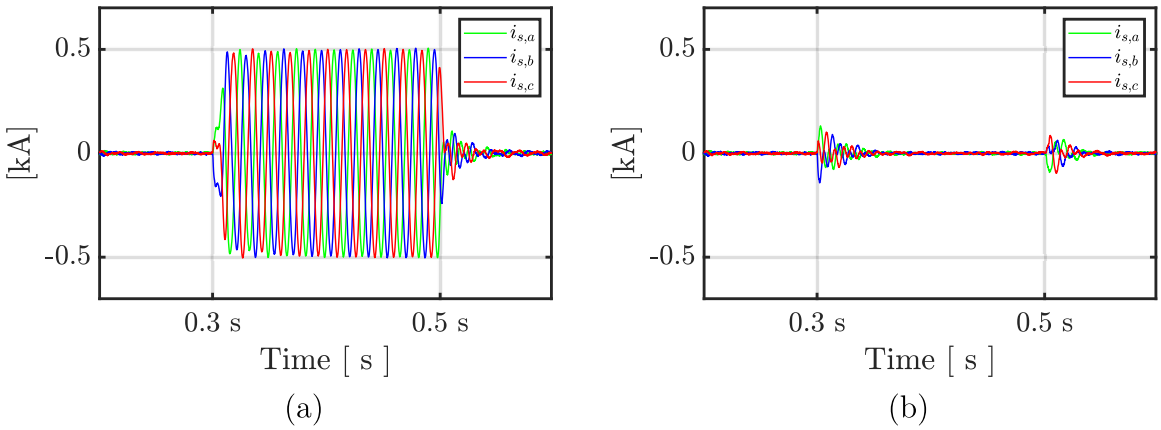


Caption: (a) With the ES-STATCOM; (b) Without the ES-STATCOM.

Source: Prepared by the author (2025).

that the currents are balanced during this brief period of time, assuming an RMS value of 353.55A with an average THD across the three phases of 0.96%. On the other hand, Figure 53(b) shows that when the ES-STATCOM is not in operation, the currents at its terminals are consequently null, exhibiting small perturbations at the critical moments related to the applied fault.

Figure 53 – Behavior of the output currents during Case C.



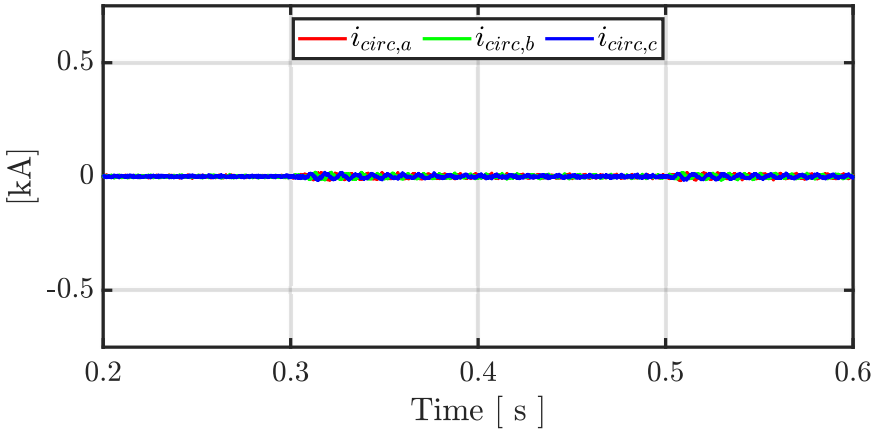
Caption: (a) With the ES-STATCOM; (b) Without the ES-STATCOM.

Source: Prepared by the author (2025).

As in the cases previously presented, the CCSC control loop was also used here to suppress the circulating currents flowing internally through the arms of the ES-STATCOM. Figure 54 shows the behavior of these currents in the three phases during the voltage support provided by the converter. It is observed that the circulating currents through the arms were completely suppressed, similarly to the previous cases. It is clear that

these currents do not affect the output currents synthesized by the ES-STATCOM, as discussed in Chapter 3. However, by maintaining a zero mean value, they contribute to the reduction of the RMS value of the current in the arms, which is eventually used in the design of the components that make up the ES-STATCOM.

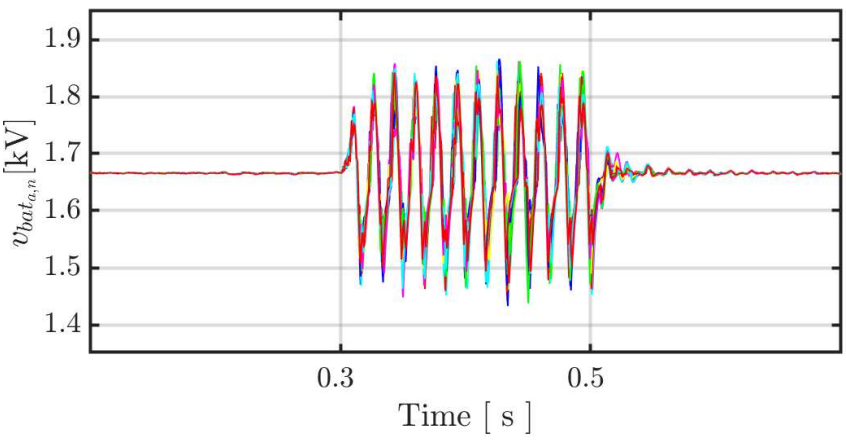
Figure 54 – Circulating currents through the ES-STATCOM arms during Case C.



Source: Prepared by the author (2025).

Finally, Figure 55 shows the voltages of the battery racks connected to the SM of the upper arm in phase "a" of the ES-STATCOM during the occurrence of the fault in the IEEE 14-bus system. It can be observed that before and after the fault, the voltages remained constant at 1.667kV. However, during the time interval corresponding to the applied symmetrical fault, 0.3 s $\leq t \leq$ 0.5 s, the voltages start to oscillate due to the operation of the ES-STATCOM for voltage support, but maintaining a mean value of 1.667kV. Note that during the pre-fault, post-fault, and fault periods, the voltages in the SM always remain equalized.

Figure 55 – Voltages of the battery racks in the upper arm of phase "a" of the ES-STATCOM during Case C.



Source: Prepared by the author (2025).

5.3 CHAPTER REMARKS

In this chapter, the effectiveness of the ES-STATCOM in providing two distinct ancillary services to the electrical grid was systematically verified through detailed simulation studies using a modified IEEE 14-bus system. The first case, Case B, demonstrated the capability of the ES-STATCOM to mitigate frequency disturbances by injecting active power in response to a significant load connection. The results confirmed that the frequency support control strategy was effective in maintaining the system frequency within acceptable limits, thereby preventing further frequency degradation. The operation of the ES-STATCOM in this scenario was characterized by well-regulated battery SoC, low harmonic distortion in the synthesized currents, and stable modulation of the battery rack voltages, confirming the robustness of both the energy storage system and the converter control architecture.

The second scenario, Case C, analyzed the voltage support capability of the ES-STATCOM during a severe symmetrical fault applied at one of the system buses. The simulations revealed that the ES-STATCOM successfully injected the maximum available reactive power, effectively supporting the voltage at the point of common coupling and reducing the voltage drop when compared to the scenario without compensation. Additionally, the converter operated with a balanced current profile, minimal harmonic distortion, and maintained equalized battery rack voltages throughout the disturbance.

In both cases, the internal circulating currents within the converter arms were fully suppressed by the CCSC control loop, ensuring safe and efficient operation of the converter components. The simulation outcomes certificated the effectiveness of the adopted control strategies in fulfilling the ancillary service requirements, while also highlighting the operational flexibility and reliability of the ES-STATCOM under distinct and challenging grid conditions.

These results consolidate the potential of the ES-STATCOM as a multi-functional device capable of enhancing both frequency and voltage stability in modern power systems with high levels of power electronic integration.

6 CLOSURE

6.1 CONCLUSIONS

This document has presented a comprehensive investigation into the modeling, control, and performance evaluation of an ES-STATCOM based on a MMC topology. The research was systematically structured across several chapters, each contributing essential insights and developments to the overall study.

In Chapter 2, the fundamental operating principles of the ES-STATCOM system were detailed. Different SM topologies and possible configurations for integrating battery systems within the BESS converter were discussed, alongside the selection of lithium-ion battery technology. Additionally, the chapter reviewed typical PWM techniques and presented a literature-based analysis of the main SoC balancing strategies. This theoretical framework established the necessary basis for the control and modeling approaches developed in the subsequent chapters.

Chapter 3 focused on the modeling and control design of the ES-STATCOM. The control strategies for both the output currents and the circulating currents were rigorously developed, considering the importance of suppressing circulating currents to improve efficiency and prevent component degradation. Additionally, the converter control mode was defined, incorporating the SoC balancing algorithm. Internal modeling details, such as the battery rack model and converter design, were also presented, ensuring that the theoretical strategies were effectively translatable to practical implementation.

The results in Chapter 4 demonstrated the performance of the ES-STATCOM under a balanced three-phase ac system. The focus was on Case A, which analyzed the SoC balancing process under different operating conditions. The simulations confirmed that SoC balancing could be effectively achieved using both active and reactive power to generate the references for the control strategies. Notably, SoC balancing using only reactive power in Case A.1 resulted in faster convergence times—approximately 585 s and 599 s, compared to 958 s and 840 s when using only active power, during discharging and charging of the batteries processes. This improvement is attributed to the efficient internal redistribution of energy within the converter without the need for net power exchange with the grid.

Additionally, a refined global SoC control strategy utilizing only active power for the SoC balancing process was introduced in Case A.2. In this scenario, the SoC values among all battery racks were initially balanced at the same time instances as in Case A.1, demonstrating the consistency and reliability of the balancing algorithm. After achieving balance, the ES-STATCOM continued operating, guiding the system towards the predefined SoC reference value. This process was successfully completed within approximately 1500 s and 1850 s. This result demonstrates that, beyond simple

balancing, the control strategy is capable of enforcing convergence toward a specific SoC target, ensuring operational flexibility and optimized battery management.

The simulations also confirmed that during all balancing processes, the suppression strategy for circulating currents was effective, ensuring low harmonic distortion and stable operation of the ES-STATCOM under the balanced grid scenario.

Chapter 5 extended the analysis to the provision of ancillary services, specifically frequency and voltage support. These services were simulated under the condition that the ES-STATCOM had already achieved a balanced SoC and equalized SM voltages. This setup was essential to assess whether, during ancillary service provision, the ES-STATCOM could maintain correct operation while preserving the balance among SoC values and SM voltages. The simulations confirmed that the control strategy successfully ensured the system's proper functionality during these ancillary services.

In Case B, the ES-STATCOM provided frequency support by injecting active power to mitigate grid frequency deviations, maintaining system stability. In Case C, the ES-STATCOM contributed to voltage support by injecting reactive power during a severe symmetrical fault, effectively reducing voltage sags and preserving the integrity of the grid connection. Importantly, during the voltage support operation, the reactive power injection exhibited a smooth behavior, free from transient peaks, which is a desirable and expected outcome. This smooth dynamic response reinforces the efficacy of the implemented control strategy.

Additionally, it is noteworthy that in all simulated scenarios, the THD of the output voltage remained well below the acceptable limits defined by international standards and Brazilian regulations. Specifically, the Module 8 of PRODIST, IEEE 519, IEC 61000-2-2, and EN 50160 establish THD limits for voltage distortion between 5% and 10%, depending on factors such as voltage level and load type. These standards focus on limiting harmonic distortions at the PCC, which can be approximated as the utility's point of energy delivery to consumers. The simulation results demonstrated that the THD values were consistently well below these regulatory thresholds, confirming the high power quality of the ES-STATCOM operation across all tested cases.

Importantly, throughout both ancillary service cases, the ES-STATCOM maintained balanced SoC values and consistent SM voltage profiles, demonstrating that the proposed control architecture not only enables effective SoC balancing but also ensures robust performance during ancillary service provision. These findings validate the overall effectiveness and robustness of the proposed control strategy under both regular SoC management and dynamic grid support operations.

In summary, the results consolidated the potential of the ES-STATCOM as a versatile and robust solution for modern power systems. These features are of strategic importance for enhancing the stability and reliability of electric power networks with high

levels of renewable energy integration. The system proved effective not only in achieving internal battery management and converter efficiency but also in providing essential ancillary services while maintaining operational stability and balance. This research lays a solid foundation for further investigations and potential real-world implementations of advanced ES-STATCOM systems in future smart grid applications.

6.2 FUTURE WORKS

Based on the context and limitations identified in this research, the following directions are suggested for future studies:

a) Implement the proposed ES-STATCOM in an experimental setup to validate the simulation results under real-world operating conditions;

b) Investigate the integration of the ES-STATCOM with different Lithium-ion battery characteristics, such as first-life and second-life batteries, to assess their impact on system performance;

c) Explore and develop optimized control strategies for the application of the proposed ES-STATCOM under unbalanced grid conditions during the SoC balancing process and the provision of ancillary services;

d) Extend the analysis to larger and more complex power systems, such as transmission networks incorporating multiple renewable energy sources, including photovoltaic and/or wind power plants, to evaluate the interoperability and control performance of the proposed ES-STATCOM;

e) Investigate and implement an offline SoC balancing methodology, performed internally without requiring the ES-STATCOM to be connected to the power grid.

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APPENDIX A – SYNCHRONOUS REFERENCE FRAME TRANSFORMATION

Park's transformation is a mathematical tool that enables the conversion of electrical quantities from the natural reference frame (NRF), which is fixed to the three-phase system (abc), to the synchronous reference frame (SRF or $dq0$), and vice versa (KRAUSE *et al.*, 2002). This transformation is particularly useful in the analysis and control of electrical machines and power converters, as it simplifies the behavior of sinusoidal quantities by converting them into steady or slowly varying signals in the rotating frame.

The transformation of quantities from the abc coordinate system to $dq0$ is given by:

$$\begin{bmatrix} f_d \\ f_q \\ f_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin(\theta) & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix}, \tag{A.1}$$

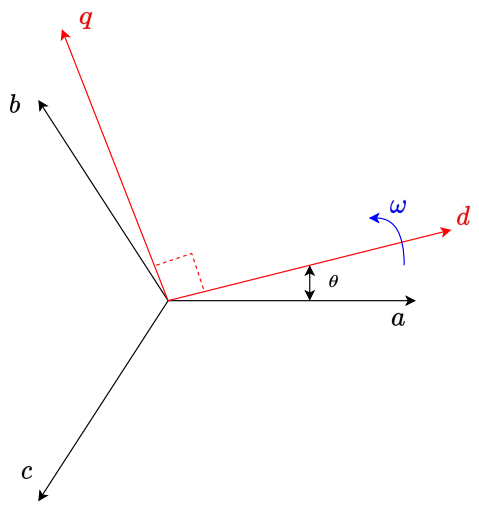
in which f_x represents the quantity to which the transformation is applied, and the factor $\frac{2}{3}$ ensures amplitude invariance of the quantities in both coordinate systems.

The inverse Park transformation, which converts quantities from $dq0$ back to abc, is given by:

$$\begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) & 1 \\ \cos(\theta - \frac{2\pi}{3}) & -\sin(\theta - \frac{2\pi}{3}) & 1 \\ \cos(\theta + \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) & 1 \end{bmatrix} \begin{bmatrix} f_d \\ f_q \\ f_0 \end{bmatrix}. \tag{A.2}$$

In Figure 56, the abc and dq coordinate systems can be seen. The angle θ is the angular difference between the d-axis and phase a, defined as $\theta = \frac{d\omega}{dt} + \theta_0$. The angular velocity of the dq reference frame is denoted by ω, and θ_0 is the initial angle value.

Figure 56 – Representation of the abc and dq coordinate systems.



Source: Adapted from Krause *et al.* (2002)

An important characteristic of Park's transformation is that the variables in the $dq0$ reference frame become continuous over time. This property is achieved when the angular velocity ω of the rotating frame is equal to the fundamental frequency of the oscillating quantities in the abc frame. Additionally, for further simplification, the initial angle θ_0 can be chosen such that one of the components, typically along either the d or q axis, is null, reducing the number of variables and simplifying the mathematical representation of the system.

APPENDIX B – DOUBLE SECOND ORDER GENERALIZED INTEGRATOR - PHASE LOCKED LOOP

The Dual Second-Order Generalized Integrator Phase-Locked Loop (DSOGI-PLL) is a robust synchronization technique widely used in power converters connected to three-phase grids. It is particularly effective under unbalanced or distorted voltage conditions, in which conventional Phase-Locked Loop (PLL) systems often fail to maintain accurate synchronization. The DSOGI-PLL architecture is composed of three main blocks: the Quadrature Signal Generator (QSG), the Positive Sequence Calculator (PSC), and a Phase-Locked Loop (PLL) that operates in the synchronous reference frame (RODRIGUEZ *et al.*, 2006).

The Quadrature Signal Generator is implemented using the Second-Order Generalized Integrator (SOGI), which processes the input voltages in the $\alpha\beta$ reference frame. Each SOGI produces two outputs: one in-phase and one in quadrature, which means 90-degree phase-shifted. The SOGI-QSG scheme is shown in Figure 57 and its transfer functions in the Laplace domain are given by:

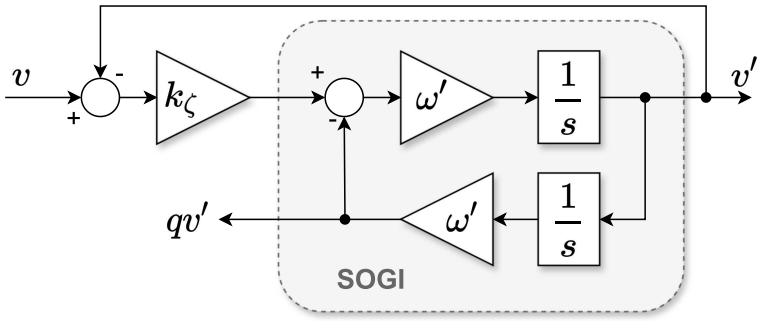
$$D(s) = \frac{v'}{v}(s) = \frac{k_\zeta \omega' s}{s^2 + k_\zeta \omega' s + \omega'^2} \tag{B.1}$$

and,

$$Q(s) = \frac{qv'}{v}(s) = \frac{k_\zeta \omega'^2}{s^2 + k_\zeta \omega' s + \omega'^2} \quad , \tag{B.2}$$

in which ω' set resonance frequency, and ζ is the damping factor of the SOGI-QSG. When $k_\zeta = \sqrt{2}$, the SOGI presents a critically damped response, providing fast convergence and limited overshoot. This value is often chosen in practical applications to balance speed and stability.

Figure 57 – Block diagram of the SOGI-QSG.

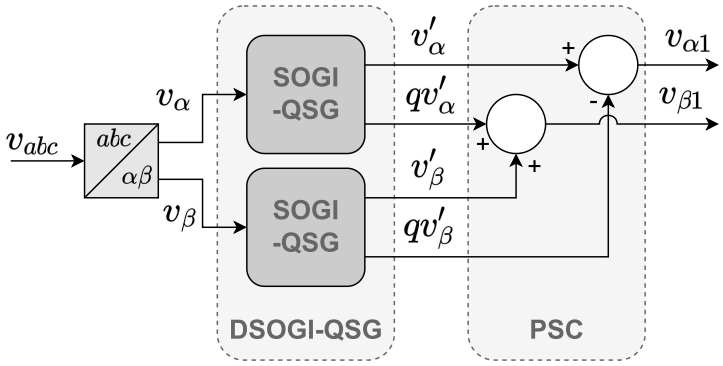


Source: Adapted from Rodriguez *et al.* (2006)

The DSOGI extends the SOGI structure to both α and β components of the grid voltage, generating four signals: v'_α, qv'_α, v'_β, and qv'_β. These signals are then used by the Positive Sequence Calculator (PSC), which isolates the positive-sequence components

of the voltage vector, as illustrates Figure 58 . The PSC is based on the instantaneous symmetrical components method applied in the $\alpha\beta$ frame.

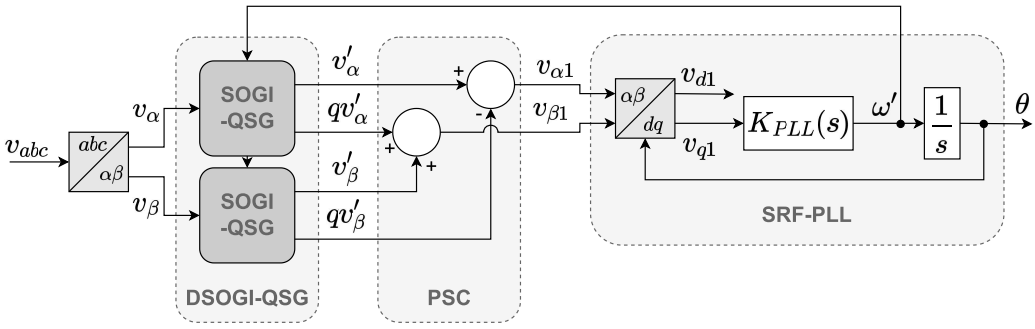
Figure 58 – Positive-sequence calculation based on DSOGI-QSG.



Source: Adapted from Rodriguez *et al.* (2006)

The extracted positive-sequence voltage components are passed through a Park transformation to obtain v_d^1 and v_q^1 in the synchronous reference frame. The PLL then regulates v_q^1 to zero using a proportional-integral (PI) controller. The controller $K_{PLL}(s)$ receives the quadrature-axis voltage and provides the estimated angular velocity ω', which, once integrated, yields the reference angle θ used for performing the Park transformations. When the controller successfully tracks the frequency, the quadrature-axis voltage will be zero, and the voltage space vector will be synchronized with the d-axis. Then, the full block diagram combining the DSOGI-QSG and the SRF-PLL is shown in Figure 59.

Figure 59 – Block diagram of the DSOGI-PLL.



Source: Adapted from Rodriguez *et al.* (2006)

The controller gains $k_{p,PLL}$ and $k_{i,PLL}$ can be designed based on the proposed by Almeida (2011), then the following expressions for the gains are obtained:

$$k_{p,PLL} = \frac{2\omega_n \xi}{V} \tag{B.3}$$

and,

$$k_{i,PLL} = \frac{\omega_n^2}{V} \quad , \tag{B.4}$$

in which ξ and ω_n are the damping coefficient and the undamped natural frequency, respectively, and V is the peak value of the inputs voltages.