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Contributions to the mitigation of voltage imbalances in modern distribution networks with modular multilevel static synchronous compensators:

modelling, control and energizing strategies

Juiz de Fora

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Orientador: Prof. Pedro Gomes Barbosa, D.Sc.

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RESUMO

Este trabalho apresenta contribuições ao controle e à operação de compensador estático síncrono trifásico baseado no conversor multinível modular para aplicações em redes elétricas modernas. Inicialmente, uma estratégia de energização é proposta para o compensador estático síncrono. O circuito de energização é composto por um controlador e dois tiristores conectados em paralelo com os contatos da chave mecânica usada para conectar o conversor à rede elétrica. Durante a primeira etapa de energização os capacitores CC dos polos positivo e negativo de duas fases do conversor são carregados com a corrente drenada da rede elétrica. O valor máximo da corrente de energização é controlado pelo ângulo de disparo dos tiristores. O modelo matemático desenvolvido permite obter uma curva característica de energização que relaciona a tensão terminal CC do conversor estático e o ângulo de disparo dos tiristores. Esta curva característica é representada por uma aproximação linear por partes para reduzir o esforço computacional do método de controle da corrente de energização. Durante as próximas etapas de energização, semicondutores específicos do conversor são comutados para que os capacitores CC dos submódulos dos outros polos do conversor recebam parte da energia armazenada nos capacitores previamente carregados durante a primeira etapa de energização. Posteriormente, malhas de controle de corrente e tensão, baseadas em modelos matemáticos no sistema síncrono de coordenadas, são apresentas para controlar o compensador estático de forma a regular a tensão de sequência positiva e compensar as tensões de sequências negativa e zero no ponto de acoplamento comum. Ainda, as malhas de controle usadas para regular a tensão terminal CC e compensar as correntes circulantes do conversor multinível modular são também apresentadas. Por último, uma metodologia de avaliação do desequilíbrio de tensão de um consumidor é apresentada e transformada para o domínio do tempo. Desta forma, as equações dinâmicas desenvolvidas são incorporadas ao controlador do compensador estático de maneira a compensar apenas os desequilíbrios de tensão de sequências negativa e zero causados pelo consumidor conectado ao ponto de acoplamento comum.

Palavras-chave: Compensador Estático Síncrono. Conversor Multinível Modular. Energização. Regulação de Tensão.

ABSTRACT

This work presents contributions to the operation and control of three-phase modular multilevel static synchronous compensators for applications in modern electric networks. Firstly, an energization strategy is proposed for the static synchronous compensator. The energizing circuit comprises a controller and two thyristors shunt-connected to the contacts of the mechanical switch used to connect the converter to the electric network. At the first energizing stage the lower and upper arm DC capacitors of two phases of the converter are charged with a current drained from the mains. The maximum value of the energizing current is controlled by the thyristors firing angle. The developed mathematical model allows to obtain an energization characteristic curve that relates the DC terminal voltage of the static converter and the thyristors firing angle. This characteristic curve is represented by a piece-wise linear approximation in order to reduce the computational effort of the energizing current control method. In the following energization stages specific converter's semiconductors are switched so that the submodule's DC capacitors of the other converter's arms receive part of the energy stored in the capacitors already charged during the first energizing stage. Posteriorly, current and voltage control loops, based on mathematical models in the synchronous reference frame, are presented to control the static compensator in order to regulate the positive-sequence voltage and to compensate the negative- and zero-sequence voltages at the point of common coupling. Moreover, control loops used to regulate the DC terminal voltage and to compensate the circulating currents of the modular multilevel converter are also presented. Lastly, a consumer voltage unbalance assessment methodology is presented and adapted to the time domain. Then, the developed dynamic equations are incorporated into the controller of the static compensator in order to compensate for only the negative- and zero-sequence voltage unbalances caused by a consumer connected to the point of common coupling.

Keywords: Static Synchronous Compensator. Modular Multilevel Converter. Energization. Voltage Regulation.

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LIST OF ABBREVIATIONS AND ACRONYMS

ANSI	American National Standard Institute
APF	Active Power Filter
CHBMC	Cascade H-bridge Multilevel Converter
DCMC	Diode-clamped (neutral-clampled) Multilevel Converter
DCSM	Double-clamp Submodule
DSCC	Double-Star Chopper Cell
DSOGI	Dual Second-Order Generalized Integrator
DSOGI-PLL	Phase-Locked Loop based on Dual Second-Order Generalized Integrator
DSP	Digital Signal Processor
DSTATCOM	Distribution Static Synchronous Compensator
FACTS	Flexible AC Transmission Systems
FCMC	Flying Capacitor Multilevel Converter
GTO	Gate Turn-off Thyristors
HB	Half-bridge
HiL	hardware-in-the-loop
HVDC	High-Voltage Direct Current
IEC	International Electrotechnical Commission
IGCT	Integrated Gate-controlled Thyristor
IGBT	Insulated Gate Bipolar Transistor
MMC	Modular Multilevel Converter
MMC-APF	Active Power Filter based on Modular Multilevel Converter
MMC-HVDC	High-Voltage Direct Current transmission system based on Modular Multilevel Converter
MMC-STATCOM	Static Synchronous Compensator based on Modular Multilevel Converter
NEMA	National Electrical Manufacturers Association
NLC	Nearst Level Control
PCC	Point of Common Coupling
PD-PWM	Phase Disposition - Pulse-Width Modulation
PI	Proportional-integral
PLL	Phase-Locked Loop
PR	Proportional-resonant
PS-PWM	Phase Shifted - Pulse-Width Modulation
PWL	Piecewise Linear
PWM	Pulse-Width Modulation
RMS	Root Mean Square

SCR	Silicon-Controlled Rectifier
SDBC	Single-Delta Bridge Cell
SHE	Selective Harmonic Elimination
SM	Submodule
SOGI	Second-Order Generalised Integrator
SRF-PLL	Phase-Locked Loop based on Synchronous Reference Frame
SSSC	Static Synchronous Series Compensator
STATCOM	Static Synchronous Compensator
SVC	Static Var Compensator
SVM	Space Vector Modulation
TVA	Tennessee Valley Authority
UPFC	Unified Power Flow Controller
VSC	Voltage Source Converter
VUF	Voltage Unbalance Factor

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1 INTRODUCTION

Three decades have passed since the concept of Flexible AC Transmission Systems (FACTS) was introduced in the late 1980's (SONG; JOHNS, 1999; HINGORANI; GYUGYI, 2000a). Although the thyristor-based Static Var Compensator (SVC) were known almost two decades before (MILLER, 1982), the seminal paper published by Hingorani (1988) was responsible for influencing the development of several topologies of static power compensators in order to obtain AC power systems with high-levels of controllability as observed in High-Voltage Direct Current (HVDC) transmission systems (ARRILLAGA; ARRILLAGA, 1998). Some examples of FACTS controllers, where the static converter controls the voltage of a power systems' bus and/or the active and reactive power flows, are the Static Synchronous Series Compensator (SSSC), the Unified Power Flow Controller (UPFC) and the Static Synchronous Compensator (STATCOM) (AKAGI; WATANABE; AREDES, 2007; HINGORANI; GYUGYI, 2000b; WATANABE *et al.*, 2018; YAZDANI; IRAVANI, 2010).

Currently, the concept of smart grids is changing the way electrical systems have been planned, operated and controlled. The use of Voltage Source Converters (VSCs) is providing more controllability and flexibility to modern electrical networks. For instance, the power system's subsystems may have different characteristic such as voltage level, frequency or number of phases. Thus, the static converters are used as interface in order to allow the energy exchange among these subsystems (MOHAN; UNDELAND, 2007; SHARKH *et al.*, 2014; YAZDANI; IRAVANI, 2010).

1.1 THE STATIC SYNCHRONOUS COMPENSATOR

The STATCOM is a high-power VSC specially designed to operate as a solid-state synchronous voltage source shunt-connected to AC transmission lines for dynamic compensation and real-time control (GYUGYI, 1993; GYUGYI, 1994). It was developed to compensate for the reactive power in its AC terminals (HINGORANI; GYUGYI, 2000b) and, its manufacture was only possible after the development of high-capacity self-commutated switches such as Gate Turn-off Thyristors (GTO), Integrated Gate-controlled Thyristor (IGCT), Insulated Gate Bipolar Transistor (IGBT), among others. When compared to its precursor SVC, based on Silicon-Controlled Rectifiers (SCRs), the STATCOM has advantages such as a faster dynamic and a lower harmonic content at its terminal voltages and currents (OGHORADA; ZHANG, 2018).

The world's first commercial STATCOM ($\pm$80 MVA/154 kV) was manufactured by Mitsubishi Electric Power Products, Inc and it was installed at Inuyama substation in Japan in 1991 to increase the stability margin of the electrical system, allowing an increase of 20% of the transmitted power through the compensated AC line (MORI *et*

al., 1993). It was built with eight sets of 10 MVA three-phase VSC, each one consisting of three single-phase converters switched at line frequency to ensure high efficiency. The output terminals of each three-phase VSC were connected in series to the other units via a zigzag transformer to generate almost sinusoidal AC voltages, without low-frequency harmonics. On the other side, the DC terminals of all units were connected in parallel to a common DC capacitor.

Four years later, in 1995, the Westinghouse Science and Technology Center commissioned the first high-power STATCOM at the Sullivan substation of the Tennessee Valley Authority (TVA) in the United States (SCHAUDER *et al.*, 1995). The ±100 Mvar/161 kV compensator was also built using eight sets of three-phase VSC which are switched on the network fundamental frequency. As in the Japanese configuration, the high number of pulses from the STATCOM ensured the generation of practically sinusoidal AC voltages so that no filter was necessary to connect it to the mains. However, the TVA STATCOM was designed to compensate for reactive power to regulate variations in the 161 kV bus voltage due to changes in load.

Currently, there are several successful STATCOM projects in operation around the world (MIHALIC; EREMIA; BLAZIC, 2016). They have the advantage of being more compact, presenting a faster response and generating less harmonics. Although they were originally proposed to enlarge the stability margin and to increase the transmission capability of electrical power systems, there are many papers where the STATCOMs are connected to distribution networks for voltage control and power factor compensation. In these applications they are commonly called Distribution Static Synchronous Compensator (DSTATCOM) (SINGH; JAYAPRAKASH; KOTHARI, 2008). One of the most relevant factors for the DSTATCOM success is the development of IGBTs able to block voltages and to switch high amplitude currents with frequencies of the order of some tens of kilohertz.

1.2 MULTILEVEL CONVERTERS

The multilevel converters are synthesized by the series or shunt connection of static converters, where the total voltage/current of the converter is distributed among the smaller converters, in a manner similar to the series/parallel connection of static switches (BRAGA; BARBI, 2000; LESNICAR; MARQUARDT, 2003). Unlike the two-level VSC the multilevel converters have the advantages of not requiring high-order harmonic filters, complex transformers or sophisticated magnetic interface structures to be connected to the mains, since its output voltages and currents are approximately sinusoidal with low harmonic content. Many multilevel converter topologies have been proposed during the last two decades (RODRIGUEZ; LAI; PENG, 2002; MALINOWSKI *et al.*, 2010; AKAGI, 2011; LUDOIS; VENKATARAMANAN, 2014). Among all of those that do not need magnetic

elements to obtain terminal voltage with multiple levels, four different main structures have been frequently reported in the literature for high-power applications: Diode-clamped (neutral-clampled) Multilevel Converter (DCMC), Flying Capacitor Multilevel Converter (FCMC), Cascade H-bridge Multilevel Converter (CHBMC), and Modular Multilevel Converter (MMC).

The DCMC has as disadvantage the fact that the number of clamping diodes required in the converter structure increases quadratically with the number of levels. In addition, as the clamping diodes require different ratings for reverse voltage blocking, the maximum number of levels of this converter is limited to seven or nine (SHARIFABADI *et al.*, 2016). The FCMC has the advantage of having redundancies for inner voltage levels, allowing the synthesis of the output voltage with different combinations of active switches. However, the large number of capacitors required makes it more expensive and bulky than the DCMC. In addition, the control of this converter with a high number of levels is more difficult. These characteristics of the DCMC and FCMC make them used in medium-voltage applications.

On the other hand, the CHBMC is better adapted for medium- and high-voltage applications, presenting several attractive features (RODRIGUEZ; LAI; PENG, 2002). Its modular structure allows to use fewer semiconductor switches to synthesize terminal voltages with the same number of levels as the previous topologies. However, in addition of requiring isolated DC sources or capacitors for each single-phase full-bridge VSC, the CHBMC's legs do not share a common DC link. This feature will force the design of larger DC capacitors.

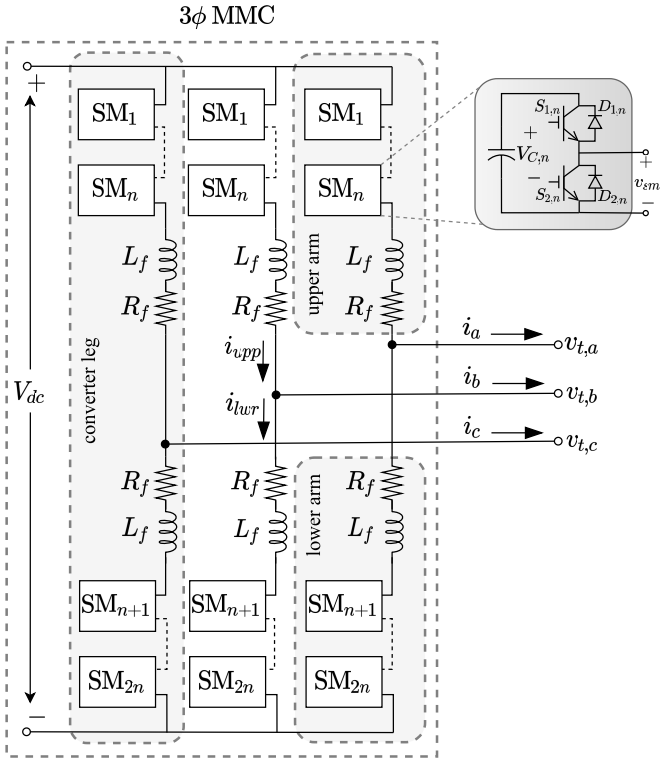
1.2.1 **Modular multilevel converter**

The MMC is one of the promising topologies in multilevel converter family, especially for medium- and high-voltage applications (AKAGI, 2011; MALINOWSKI *et al.*, 2010; LUDOIS; VENKATARAMANAN, 2014; DU *et al.*, 2018; RODRIGUEZ; LAI; PENG, 2002; DAS; NADEMI; NORUM, 2011; LESNICAR; MARQUARDT, 2003; DEBNATH *et al.*, 2015). Due to its capacity to synthesize low distorted voltages, while the switching losses are kept lower than other multilevel converter topologies, the MMC have been used also to drive medium-voltage motors (DU *et al.*, 2018), to integrate large wind and solar power plants into the grid (SHARIFABADI *et al.*, 2016) and to operate as active power filter (GHETTI *et al.*, 2012) and static synchronous compensator (ORCAJO *et al.*, 2020; DUARTE *et al.*, 2019). Moreover, the MMC have been gained a lot of attention in recent years due to their scalability and the fact that they do not need isolated DC sources, since the DC terminal voltage is shared between several series connected submodules (SMs) (DU *et al.*, 2018).

Diagram 1 shows a schematic diagram of the three-phase MMC. Each arm of the

converter is composed by n series-connected SMs, based on a Half-bridge (HB) converter topology comprising two semiconductor switches and one DC capacitor. On the other hand, each leg is formed by one upper arm and one lower arm. Other topologies of converters with a larger number of semiconductor switches, such as the full-bridge or double-clamp converter, can also be used in the SM structure (ABILDGAARD; MOLINAS, 2012; XUE; XU; TANG, 2014). Despite some advantages of using these alternative topologies, as the capacity of interrupting short-circuit currents at its DC terminals (XUE; XU; TANG, 2014), the greater number of switches increases the complexity and switching losses of the converter. Although other semiconductor switches can be used to compose the SM, the IGBT is commonly adopted. Due to the modular topology of this converter the number of levels are directly proportional to the number of series-connected SMs. Another advantage related to its modularity, is the SM redundancy and ease of maintenance. In Diagram 1, the parameters L_f and R_f are the inductance and resistance of the passive filter used to connect the MMC arms to the AC output terminals. V_{dc} is the DC terminal voltage, $v_{t,abc}$ and i_{abc} are the AC terminal voltages and currents, respectively, and i_{upp} and i_{lwr} are the upper and lower arm currents.

Diagram 1 – MMC schematic diagram.



Source: Elaborated by the author (2021).

Some of the advantages of the MMC, compared to the other topologies of VSC, are summarized bellow (ABILDGAARD; MOLINAS, 2012; ALLEBROD; HAMERSKI; MARQUARDT, 2008; KIM; LEE; HAN, 2017; LESNICAR; MARQUARDT, 2003; OGHO-

RADA; ZHANG, 2018; XUE; XU; TANG, 2014):

- The DC terminal voltage is distributed among the SMs of the MMC;
- No insulated DC sources are required for the case in which the MMC injects power into the electric network;
- The passive filters used as interface with the grid are smaller due to the multilevel terminal voltages with lower harmonic content;
- The rated voltage of the MMC can be increased by adding more SMs in its structure;
- The MMC can be switched with low frequency so that the switching power losses are low;
- The converter has higher reliability due to the possibility of insertion of redundant SMs;
- As the voltages across the SM switches is lower, the series-connection of switches are not required, avoiding problems related to the simultaneous switching.

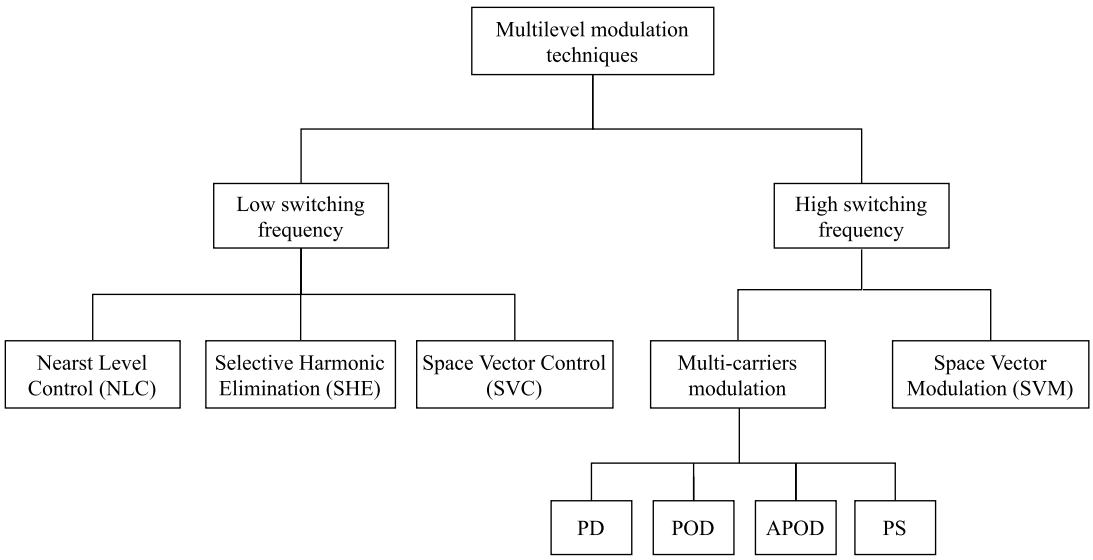
1.2.2 **Basic switching control techniques**

There are several switching control techniques proposed in the literature for the multilevel converters. These techniques can be divided in two groups: low-frequency and high-frequency switching. The main low-frequency switching techniques are the Nearst Level Control (NLC), Selective Harmonic Elimination (SHE) and Space Vector Control (SVC) (FRANQUELO *et al.*, 2008). These techniques are more appropriate for high-power applications such as HVDC transmission systems, in order to ensure low switching losses. On the other hand, the high-frequency switching techniques are the Space Vector Modulation (SVM) and multi-carrier Pulse-Width Modulation (PWM). The SVM is more common in applications such as motor drive systems while the multi-carrier PWM is the most used switching technique for the MMC. The main types of multi-carrier switching techniques are the Phase Shifted - Pulse-Width Modulation (PS-PWM) and Phase Disposition - Pulse-Width Modulation (PD-PWM). Figure 1 shows the main types of modulation techniques for multilevel converters (GHETTI, 2019).

In the multicarrier PWM technique several high-frequency triangular waveform carriers are compared with the same reference signal. The number of carriers should be the same number of SMs per arm n. Then, the binary resulting signals can be used to control the respectively switches of the MMC's submodules.

In the PS-PWM technique n carriers with the same amplitude, however phase-shifted by $\phi = 360°/n$, are compared with a reference signal. If the n carriers related to the upper arm of the MMC are phase-shifted by $\phi_d = 360°/2n$ from the carriers related to

Figure 1 – Modulation techniques for multilevel converters.



Source: Adapted from (GHETTI, 2019).

the lower arm, the phase-voltage at the converter terminals will present $(2n + 1)$ levels. However, if $\phi_d = 0$, the phase-voltage at the converter terminals will present $(n + 1)$ levels.

In the PD-PWM technique n carriers with the same phase and amplitude are used, however they are displaced by a DC level. If the carriers related to the upper arm of the MMC are in phase with the carriers related to the lower arm, the phase-voltage at the converter terminals will present $(2n + 1)$ levels. On the other hand, if the carriers related to the upper arm of the MMC are 180° phase-shifted with the carriers related to the lower arm, the phase-voltage at the converter terminals will present $(n + 1)$ levels.

It is important to mention that the greater the number of levels of the converter the lower the harmonic content of the waveforms. However, for a phase-voltage with $(n + 1)$ levels the number of active SMs in a MMC's leg is always equal to n. On the other hand, for a phase-voltage with $(2n + 1)$ levels the number of active SMs in a MMC's leg vary between $(n - 1)$ and $(n + 1)$ causing an increase in the high-frequency ripple of the MMC DC terminal voltage (SAEEDIFARD; IRAVANI, 2010). Moreover, for a phase-voltage with $(2n + 1)$ levels the equivalent capacitance seen from the DC-side vary while for a phase-voltage with $(n + 1)$ levels the equivalent capacitance is constant. Therefore, the choice of the switching control technique for the MMC should consider all its advantages and disadvantages.

1.2.3 MMC SM voltage equalization

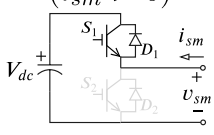
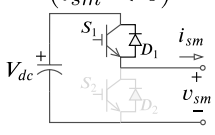
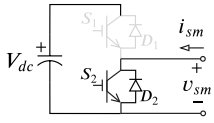
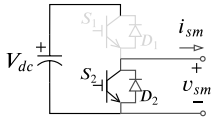
The voltages of the SM capacitors must be regulated since the DC terminal voltage controller is not able to perform this task. Two approaches are commonly proposed in the literature to equalize the voltages of the SM capacitors. The first technique involves the

design of individual controllers to regulate the voltages of each SM (HAGIWARA; AKAGI, 2009). This choice has the disadvantage that it cannot be implemented in MMC with a large number of SMs since it would be necessary to use many independent measurement and control loops. The second strategy uses an algorithm to rank the SMs, in ascending or descending order, according to their capacitor voltages. Subsequently, the algorithm determines which SMs should be activated or bypassed (SAEEDIFARD; IRAVANI, 2010).

Table 1 shows four different operation modes for the half-bridge SM. The colored line indicates the path of the current through the semiconductor switches and the DC capacitor. Depending on whether the current i_{sm} is positive or negative, the DC capacitor will be charged or discharged when the SM status is the Insert Mode, respectively. Otherwise, when the half-bridge operates in Bypass Mode, the DC capacitor is disconnected from the SM output terminals.

The MMC voltage equalization algorithm determines at each moment the number of SMs that must be inserted in the upper (m_{upp}) and lower (m_{lwr}) arms of each leg of the MMC (SAEEDIFARD; IRAVANI, 2010; DARUS *et al.*, 2014; GHETTI *et al.*, 2017). So depending on whether the current through the upper and lower arms is positive or negative, the equalization algorithm will select the SMs with the least and most charged capacitors to be inserted, respectively. Thus, if the current through the MMC arm is positive, the algorithm will insert the SMs which capacitors are least charged, so they will be charged. On the other hand, if the current through the arm is negative, it will select the SMs which capacitors are overcharged, so they will be discharged.

Table 1 – Operation modes for the half-bridge SM.

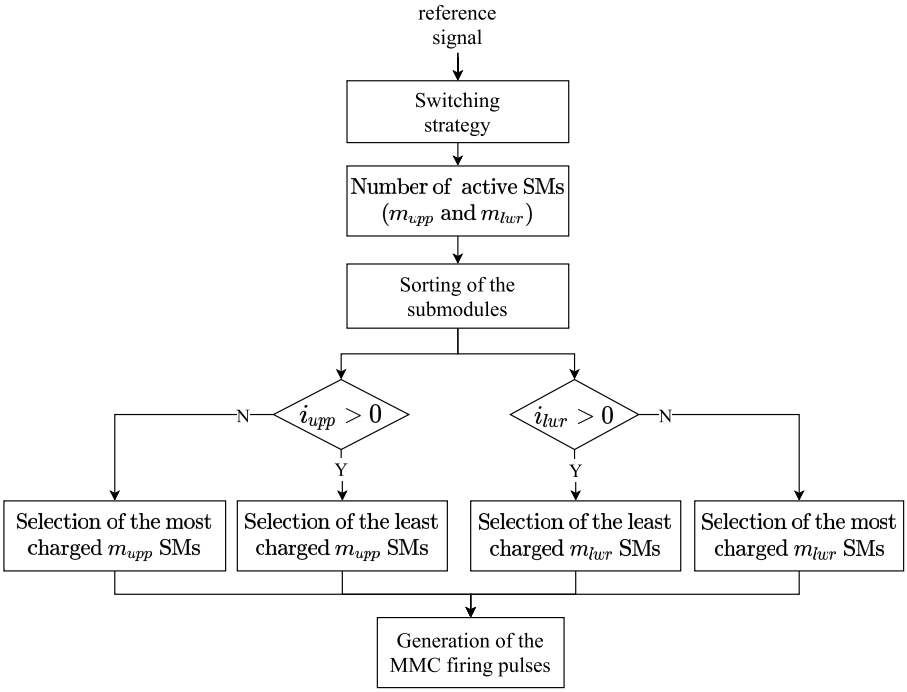
Insert Mode (S_1 active & S_2 blocked)	
$(i_{sm} > 0)$	$(i_{sm} < 0)$
	
Bypass Mode (S_1 blocked & S_2 active)	
$(i_{sm} > 0)$	$(i_{sm} < 0)$
	

Source: Reproduced from (DUARTE; ALMEIDA; BARBOSA, 2020).

From the above, the voltage equalization algorithm plays an important role in the operation of the MMC. That is, it must be accurate and fast enough to measure and sort

all SMs, according to the voltages of their capacitors, before the next switching of the MMC. Flowchart 1 illustrates the voltage equalization algorithm proposed in (GHETTI *et al.*, 2017) for the MMC. The authors compared the performance of six different sorting algorithms to equalize the SM voltages of a MMC. They were implemented in a Digital Signal Processor (DSP) and used to regulate the voltages of a real-time model of MMC embedded in a hardware-in-the-loop (HiL) platform. Although all tested algorithms could perform the task with no problems, the algorithm based on the Shell method presented one of the best performances when a large number of SMs was considered.

Flowchart 1 – Flowchart of the SM voltage equalization algorithm.



Source: Adapted from (GHETTI, 2019).

1.2.4 **MMC circulating currents**

An important issue related to the MMC is the control of circulating currents. These currents arise between the upper and lower arms of each leg of the MMC due to imbalances in the DC voltages of the SMs' capacitors. Although the circulating currents are formed by negative-sequence harmonic components multiple of the grid frequency, they consists mainly of second-order harmonics and have no impact on the AC output voltages and currents. They cannot be completely eliminated. However through a proper control, some undesired effects, such as increase in the semiconductors switches power loss and higher voltage ripple on the SM capacitors, can be minimized or even suppressed. Different circulating current control techniques were proposed in the literature, including the use of Proportional-integral (PI), resonant and Proportional-resonant (PR) controllers,

as shown in (TU; XU; XU, 2011; DEBNATH *et al.*, 2015; LI *et al.*, 2013; CUPERTINO *et al.*, 2018b).

1.3 MOTIVATION

As the MMC has one of the converter topologies most suitable for medium- and high-voltage applications, several control techniques and energization strategies were proposed for this converter in the last decade.

Although the mathematical modellings, in the synchronous reference frame, to derive the positive-sequence voltage control loop of the STATCOM to regulate the voltage at the Point of Common Coupling (PCC) are already presented in the literature (YAZDANI; IRAVANI, 2010), the same can not be said for the negative- and zero-sequence voltage control loops used to compensate the voltage imbalance at the PCC. Although there are works in the literature were static converters are used for voltage imbalance compensation in power systems, a mathematical model for the negative- and zero-sequence voltage compensation at the PCC is not presented, and consequently, the gains of the compensator's controllers cannot be designed.

On the other hand, the majority of the energization strategies presented in the literature for the MMCs are based on the use of current limiting resistors which need auxiliary bypass mechanical switches and may be expensive depending of the rating of the converter. Moreover, the use of these resistors during the pre-charge of the converters' DC capacitors does not allow to control the energizing current. Thus, in addition to the peak value not being constant the current is only limited.

Moreover, several researchers have proposed consumer imbalance assessment methodologies in the last decade in order to identify the contribution of the consumer for the voltage imbalance at the point of common coupling. However, the majority of the methodologies are presented in steady-state, which is not suitable to be implemented in real-time applications such as the STATCOM. Thus, the next section will present the goals defined for this work.

1.4 WORK GOALS

The objective of this thesis is not to solve all the problems involving the use of modular three-phase converters, with three and four wires, as distribution static synchronous compensators, but to report some challenges and solutions related to the operation and control of a Static Synchronous Compensator based on Modular Multilevel Converter (MMC-STATCOM) connected to modern distribution networks. Then, the following topics were defined as goals for this work:

a) to model, in an electromagnetic transient program, a MMC-STATCOM with 28 SMs per leg connected to a 24 kV distribution network;

b) to propose an energization strategy, based on semiconductor switches (thyristors), for the MMC-STATCOM;

c) to develop mathematical models to control the firing angles of the energization circuit's thyristors in order to regulate/limit the energizing current of the MMC-STATCOM;

d) to present digital simulation results in order to demonstrate and to validate the proposed energization strategy;

e) to develop mathematical models to derive positive-, negative- and zero-sequence current and voltage control loops for the MMC-STATCOM in order to regulate the positive-sequence voltage and to compensate the negative- and zero-sequence voltages at the PCC;

f) to develop a consumer voltage imbalance assessment methodology, in the time domain, to be embedded in the controller of the MMC-STATCOM to generate references for the negative- and zero-sequence PCC voltage control loops of the static compensator in order to compensate only the parcel of voltage imbalance caused by a consumer connected at the PCC;

g) to present digital simulation results in order to demonstrate the performance and to validate the current and voltage control loops of the MMC-STATCOM as well as the consumer voltage unbalance assessment methodology.

1.5 CONTRIBUTION OF THIS THESIS

As a result of the investigations, this thesis brings the following contributions to the research field of modular multilevel converters (power electronics) and compensation for imbalance of modern electrical networks (microgrids):

i) A novel strategy to energize a MMC-STATCOM from its AC-side terminals without using additional resistors, inductors, transformer or DC auxiliary source. The proposed strategy is divided into four energizing stages and does not require any topological change to be implemented. The proposed methodology also presents the advantage of being easily expandable for MMCs with any number of SMs and for any grid voltage.

ii) An improvement of the energization strategy previously proposed, where the charging process can also be used to pre-charge three-phase three-wire or four-wire MMCs unlike the previous method, that could only be used for three-phase three-wire converters. In addition, the upper and lower arms of the MMC are

not connected in series in the last energization stage, avoiding an overvoltage in the DC terminals of the converter.

iii) A broad description of the controller design steps of a MMC-STATCOM to compensate the positive- and negative-sequence voltages of an unbalanced distribution network. Linearised mathematical models are used to derived positive- and negative-sequence transfer functions in order to design of the MMC's controllers in the frequency domain.

iv) A strategy to control a three-phase four-wire MMC-STATCOM to compensate for zero-sequence voltage imbalances of the electric network. A synchronous-dq frame mathematical modelling is used to derive the positive- and zero-sequence control loops for the static compensator. The compensator is controlled to synthesize currents in order to regulate the positive-sequence voltage at the PCC. The fourth-leg of the MMC-STATCOM is controlled as a single-phase converter to compensate the zero-sequence voltage at the PCC.

v) A methodology to quantify, in the time-domain, the voltage unbalance parcels at the PCC due to the utility system (supplier) as well as the one due to the consumer (load). The methodology proposed here will be used to control a MMC-STATCOM to compensate only the imbalance generated by the consumer, avoiding the compensation of all the negative- and zero-sequence voltages at the PCC. This strategy allows also to reduce the capacity of the compensator.

1.6 SCIENTIFIC PRODUTION OF THIS THESIS

In addition to previous contributions, the following works were published and submitted to scientific journals, conferences and publishers, with the results of research carried out during this doctorate[1]:

a) Papers published in scientific journals:

[1] DUARTE, S. N.; GHETTI, F. T.; ALMEIDA, P. M.; BARBOSA, P. G. Experimental evaluation of negative-sequence voltage compensation in distribution networks by a modular multilevel static synchronous compensator. **Electric Power Systems Research**, Elsevier, v. 194, 2021.

[2] DUARTE, S. N.; ALMEIDA, P. M.; BARBOSA, P. G. Enhancing the performance of pre-charging strategy of a modular multilevel static synchronous compensator. **Journal of Control, Automation and Electrical Systems**, Springer, p.1–11, 2020.

[3] DUARTE, S. N.; SOUZA, B. C.; ALMEIDA, P. M.; ARAUJO, L. R.; BARBOSA, P. G. Control algorithm for DSTATCOM to compensate consumer-

[1] Click on the title to access the most relevant works.

generated negative and zero sequence voltage unbalance. **International Journal of Electrical Power & Energy Systems**, Elsevier, v. 120, p. 105957, 2020.

[4] DUARTE, S. N.; SOUZA, B. C. de; ALMEIDA, P. M. de; ARAÚJO, L. R. de; BARBOSA, P. G. A compensation strategy based on consumer's voltage unbalance assessment for a distribution static synchronous compensator. **IEEE Latin America Transactions**, IEEE, v. 18, n. 01, p. 156–164, 2020.

[5] DUARTE, S. N.; ALMEIDA, P. M.; BARBOSA, P. G. A novel energizing strategy for a grid-connected modular multilevel converter operating as static synchronous compensator. **International Journal of Electrical Power & Energy Systems**, Elsevier, v. 109, p. 672–684, 2019.

[6] DUARTE, S. N.; GHETTI, F. T.; ALMEIDA, P. M. de; BARBOSA, P. G. Zero-sequence voltage compensation of a distribution network through a four-wire modular multilevel static synchronous compensator. **International Journal of Electrical Power & Energy Systems**, Elsevier, v. 109, p. 57–72, 2019.

[7] DUARTE, S. N.; FOGLI, G. A.; ALMEIDA, P. M.; BARBOSA, P. G. Energization and de-energization strategies of a DSTATCOM. **Brazilian Journal of Power Electronics**, SOBRAEP, v. 23, n. 1, p.29–38, March 2018.

b) Papers submitted for scientific journals:

[1] DUARTE, S. N.; ALMEIDA, P. M.; BARBOSA, P. G. Voltage regulation of a remote microgrid bus with a modular multilevel static synchronous compensator. **International Journal of Electrical Power & Energy Systems**, Elsevier, 2021.

c) Book chapter in production process:

[1] DUARTE, S. N.; BARBOSA, P. G.; KABALCI, E. **Multilevel inverters: STATCOM and D-STATCOM with multilevel inverters**. [S.l.]: Elsevier.

d) Papers presented in technical conferences:

[1] DUARTE, S. N.; SOUZA, B. C.; ALMEIDA, P. M.; ARAÚJO, L. R.; BARBOSA, P. G. Performance of a multi-grounded distribution network with a four-wire three-phase power conditioner. In: IEEE. **2019 IEEE 15th Brazilian Power Electronics Conference and 5th IEEE Southern Power Electronics Conference (COBEP/SPEC)**. [S.l.], 2019. p. 1–6.

[2] DUARTE, S. N.; SOUZA, B. C.; ALMEIDA, P. M.; BARBOSA, P. G. Voltage regulation of a remote bus of a distribution network by static

synchronous compensator. In: IEEE. **2019 IEEE 15th Brazilian Power Electronics Conference and 5th IEEE Southern Power Electronics Conference (COBEP/SPEC)**. [S.l.], 2019. pp. 1–6.

[3] SOUZA, B. C.; DUARTE, S. N.; ALMEIDA, P. M.; BARBOSA, P. G.; ARAÚJO, L. R. A new zero-sequence voltage compensation algorithm for a dstatcom based on consumer unbalance. In: IEEE. **2019 IEEE 15th Brazilian Power Electronics Conference and 5th IEEE Southern Power Electronics Conference (COBEP/SPEC)**. [S.l.], 2019. p. 1–6.

[4] BRAGA, M. F.; DUARTE, S. N.; SOARES, G. M.; BARBOSA, P. G. Design method to reduce the DC link voltage of a three-wire three-phase hybrid active power filter. In: IEEE. **2019 IEEE 15th Brazilian Power Electronics Conference and 5th IEEE Southern Power Electronics Conference (COBEP/SPEC)**. [S.l.], 2019. p. 1–6.

[5] DUARTE, S. N.; ALMEIDA, P. M.; BARBOSA, P. G. Zero-sequence network voltage compensation by a three-phase four-wire grid-connected converter. In: IEEE. **2018 Simpósio Brasileiro de Sistemas Elétricos (SBSE)**. [S.l.], 2018. p. 1–7.

[6] BRAGA, M.; DUARTE, S.; ALMEIDA, P.; BARBOSA, P. DC capacitor energization and voltage regulation of a single-phase hibrid filter. In: IEEE. **Brazilian Power Electronics Conference (COBEP)**. [S.l.], 2017. p. 1–6.

[7] DUARTE, S. N.; ALMEIDA, P. M. de; BARBOSA, P. G. Grid connected voltage-source converter pre-energization strategy. In: IEEE. **2017 Brazilian Power Electronics Conference (COBEP)**. [S.l.], 2017. p. 1–5.

e) Paper submitted for conference:

[1] DUARTE, S. N.; ALMEIDA, P. M.; BARBOSA, P. G. Voltage compensation in multi-grounded distribution network with a three-phase five-wire DSTATCOM. **International Conference on Power Systems Transients (IPST)**, 2021.

1.7 ORGANIZATION OF THIS THESIS

Besides Chapter 1, this thesis contains five more chapters, each based on one of the journal papers published by the author and indicated in Section 1.6. Therefore, each chapter will present a bibliographic review associated with the topic to be addressed, the mathematical modelling and the design of controllers used to regulated the voltages and currents synthesized by MMC-STATCOM as well as results of the digital simulations. In this way, the next chapters are organized as follows:

Chapter 2 presents the energizing circuit for the MMC-STATCOM. Each energizing stage is mathematically modelled so that the energizing current drained from the mains can be controlled and the energy stored in the DC capacitors during the first stage can be distributed to all the submodule DC capacitors of the MMC-STATCOM. Digital simulation results are also presented to demonstrate and to validate the proposed energizing strategy.

Chapter 3 presents the MMC-STATCOM regulating the positive-sequence voltage and compensating the negative-sequence voltage at the PCC. The current and voltage control loops of the three-phase three-wire MMC-STATCOM are designed in the synchronous reference frame. A Dual Second-Order Generalized Integrator (DSOGI) is used to extract the negative-sequence component of the PCC voltages. The control loops to regulate the DC terminal voltage and to compensate the circulating currents of the MMC-STATCOM are also presented. Digital simulation results are used to demonstrate and to validate the negative-sequence voltage compensation strategy and the design of the MMC-STATCOM controllers.

Chapter 4 presents the current and voltage control strategy, in the synchronous reference frame, for a three-phase four-wire MMC-STATCOM. The fourth-leg of the MMC-STATCOM is controlled as a single-phase converter to compensate the zero-sequence voltage at the point of common coupling. The Second-Order Generalised Integrator (SOGI) and a buffer circuit are used to generate a fictitious β-component for the voltage at the PCC and the current synthesized by the MMC-STATCOM, respectively. Digital simulation results are also presented to demonstrate and to validate the zero-sequence voltage compensation strategy and the design of the MMC-STATCOM controllers.

Chapter 5 presents a consumer voltage unbalance assessment, in the time domain, so that the MMC-STATCOM can compensate for only the voltage unbalance parcel caused by a consumer connected to the PCC. Digital simulation results are also presented to demonstrate and validate the methodologies proposed.

Finally, Chapter 6 presents the final conclusions of this work and proposals for future works.

In addition to the previous chapters, four Appendices present the main parameters of the electrical networks, MMC-STATCOMs, controllers and digital filters used in digital simulations whose results are presented in Chapter 2, Chapter 3, Chapter 4 and Chapter 5.

2 A NOVEL ENERGIZING STRATEGY FOR A GRID-CONNECTED MMC OPERATING AS STATCOM

This chapter presents a strategy to smoothly charge the MMC-STATCOM DC capacitors in order to avoid inrush currents through the semiconductor switches of the compensator (DUARTE; ALMEIDA; BARBOSA, 2019). Subsequently, a second paper on the theme was published with an improvvement on original strategy proposed (DUARTE; ALMEIDA; BARBOSA, 2020).

2.1 INTRODUCTION

Regardless of the VSC topology, multilevel or not, when its DC capacitors are discharged it can not be connected to the grid without an energization strategy. Otherwise, a high amplitude uncontrolled current is drained from the mains flowing through the diodes of the converter's switches. As this current is limited only by the converter's passive filters and the network impedance, it can damage the switches and filters of the converter, besides to cause malfunction in protection circuits and interference in electronics equipment (LARSSON; THORVALDSSON; AKESSON, 2002; LESNICAR; MARQUARDT, 2004; MANOLAROU; KOSTAKIS; MANIAS, 2005; PETRY, 2012; SHI *et al.*, 2012). This initial period of the energizing process is called pre-charge of the converter.

Notwithstanding, the energization of the VSCs is not a well explored and documented subject in the literature when compared to its normal operation mode (HAN, 2006; KIM; LEE; HAN, 2017; SHI *et al.*, 2012; XUE; XU; TANG, 2014). In most of the works it is considered that the DC capacitors are already charged or resistors and inductors are used to limit the energizing current drained from the grid (CHAVES, 2007; PINTO, 2010; ROCHA; ARAÚJO; NOVAIS, 2003). However, depending on the values of the inductance and operation current, the weight and volume of a reactor may be a disadvantage (MANOLAROU; KOSTAKIS; MANIAS, 2005). In the case of using resistors, besides the energy being dissipated, the use of high capacity thermal resistors may be necessary, mainly in high power applications (XUE; XU; TANG, 2014).

Several energizing strategies for two and three-level static converters are presented in (BRAGA *et al.*, 2017; DUARTE, 2017; DUARTE *et al.*, 2018; LARSSON; THORVALDSSON; AKESSON, 2002; RIBEIRO *et al.*, 2014). For the case of the MMC, regardless of the topology adopted, the SM capacitors of the MMC also drain high currents from the mains when they are discharged (DUARTE; ALMEIDA; BARBOSA, 2019). Thus, depending on where the converter is connected, different energizing strategies, both on the AC- and DC-side, were proposed and published in the literature at the last decade (KIM; LEE; HAN, 2017; SHI *et al.*, 2012; XUE; XU; TANG, 2014).

In (LESNICAR; MARQUARDT, 2003) and (LI; ZHAO, 2010) the authors use

an auxiliary power supply to charge, one by one, the SM capacitors of a MMC. The DC power supply is connected to the MMC terminals through additional mechanical switches. The output voltage of this auxiliary power supply should also vary from zero to the rated capacitor voltage of the SM. In (LI; ZHAO, 2010), the converter's inductors are also short-circuited by additional mechanical switches to avoid the energy exchange with the capacitors of the MMC. Despite the simplicity, this method is not practical for medium- and high-voltage applications where the number of SMs of the MMC is high (LI *et al.*, 2015). A similar strategy is proposed in (XU *et al.*, 2011). However, besides the needing of a DC power supply, four thyristors are connected to each SM. These switches are triggered in synchronism to simultaneously charge all DC capacitors of the MMC up to their nominal value. Due to the high number of switches, the cost of this energizing circuit is further increased. In (TIAN *et al.*, 2016) a pre-charge scheme reconfigures the semiconductor switches of the SMs to operate as a boost converter. In addition to the need for the DC power supply, this method has limitations associated with the maximum duty cycle ratio for the operation of the boost converter.

Alternatively, it is possible to avoid the use of the auxiliary DC power supply in applications where the MMC drives high-power motors or process the energy from HVDC transmission systems (ZHANG *et al.*, 2017; XUE; XU; TANG, 2014). In this case the SM capacitors can be charged by the rectifier connected to the DC-side of the MMC. However, current limiting resistors are frequently used to limit the inrush current drained from the mains, since the SM's diodes of the MMC allow the current flow even if all converter's switches are blocked (ZHANG *et al.*, 2017). For instance, in (XUE; XU; TANG, 2014) resistors are series-connected to the mains to limit the energizing current of a Double-clamp Submodule (DCSM) based MMC of an HVDC transmission system.

On the other hand, several energization strategies where proposed in the literature for applications in which the MMC is parallel-connected to the network as a STATCOM or an Active Power Filter (APF). In these applications, the SM capacitors of the inverter can be charged by absorbing power directly from the AC network. In (LIU *et al.*, 2013; YANG *et al.*, 2013; DAS; NADEMI; NORUM, 2011) the authors connect additional resistors in series with the arm inductors of the MMC to limit the inrush current drained from the mains. On the other hand, in (SHI *et al.*, 2012) the energizing current drained by the capacitors of a MMC is limited by a bank of resistors series-connected to the AC network. In addition to the fact that the current is not controlled, this scheme may face problems in high-voltage/power applications, since high-thermal capacity resistors will be required. Besides the power losses, these resistors are expensive and should be bypassed by additional mechanical switches after the energization of the converter (XUE; XU; TANG, 2014; SHI *et al.*, 2015).

As in the previous works, in (LI *et al.*, 2014; LI *et al.*, 2015; LIU *et al.*, 2019a; LIU *et al.*, 2019b; BISSAL; ALI, 2019; WANG *et al.*, 2020) the authors also use resistors to limit

the uncontrollable current drained from the AC- or DC-side, depending on the application of the MMC. However, these works focus on the control of the energizing current after the pre-charge of the SM capacitors. For comparison purposes, the current-limiting resistors used in (LIU *et al.*, 2019a) have a value of 3 kΩ, that is, approximately 105 times the filter impedance value of each arm of the MMC which is 28.3 Ω (75 mH). In (WANG *et al.*, 2020) it is presented an unified start-up strategy for MMCs using a closed-loop control scheme where the conventional controller design and parameter tuning are not necessary. The SM capacitors can be charged from either AC- or DC-side mains voltages. However, in both cases, the current limiting resistors are still needed and additional mechanical switches are also required to bypass the resistors.

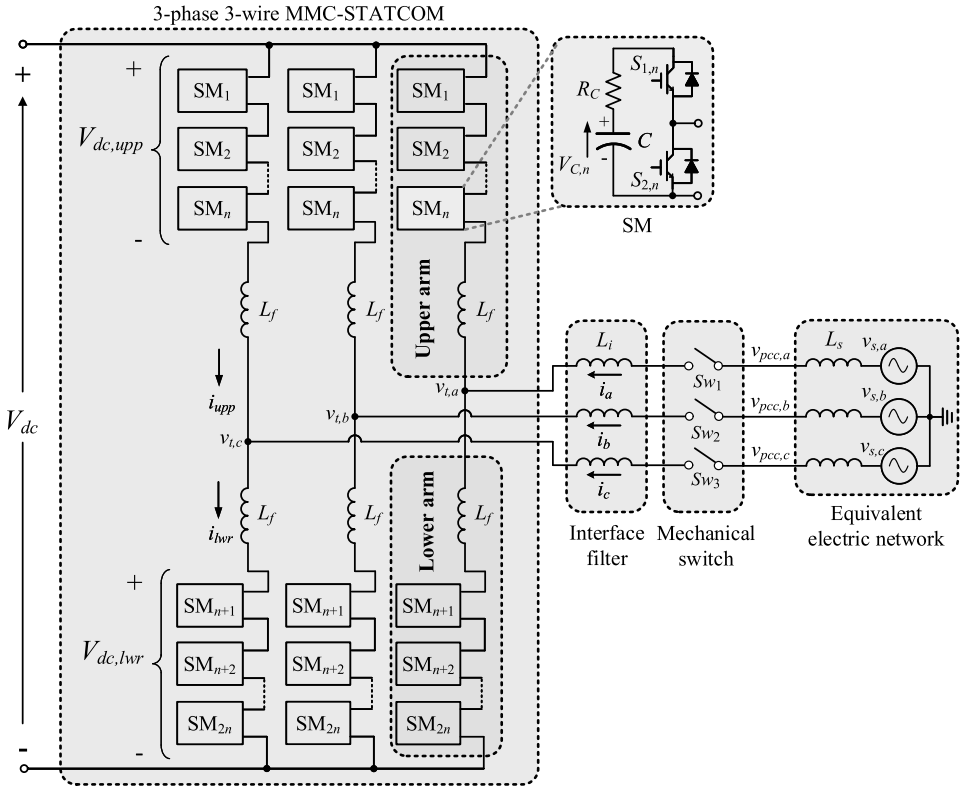
Thus, one of the objectives of this thesis is to present an energizing strategy for a static synchronous compensator based on the modular multilevel converter. Different from others strategies presented in the literature, no resistors, inductors, transformers, DC power supply or additional mechanical switches are used in the proposed strategy. The energizing circuit is composed by two thyristors parallel-connected with the mechanical switch used to connect the static compensator to the mains. Thus, no topological changes are made in the MMC-STATCOM to charge the DC capacitors of the SMs. During the first stage, the SM capacitors of two phases of the converter are charged by the energizing current drained from the AC network. During this stage, the energizing current is controlled by the firing angle of the thyristors. In the next energizing stages, the energy of the capacitors charged during the first stage is distributed to the other SM capacitors by activating specific switches of the converter. The energization stages are sequentially repeated until the DC voltages of the SMs reach $\sqrt{2}V_{s,ab}/n$, where $V_{s,ab}$ is the Root Mean Square (RMS) line-to-line voltage of the mains and n is the number of SMs per arm of the MMC-STATCOM. Each energizing stage is mathematically modelled and used to derive a control law for the energization circuit. The method is also suitable for MMCs with any number of SMs per arm.

2.2 THE MMC-STATCOM

Diagram 2 shows the schematic diagram of the three-wire three-phase MMC connected to an equivalent electric network as MMC-STATCOM. For the sake of simplicity, in this diagram the intrinsic resistances of the inductors were omitted. The power system is modelled by a three-phase voltage source connected in series with three impedances $(R_s + \jmath\omega_s L_s)$. Three first-order low-pass filters, composed of an inductance L_i and its intrinsic resistance R_i, are used as interface between the converter and the grid. Each arm of the MMC-STATCOM is formed by n series-connected SMs. The upper and lower arms of each leg of the MMC are connected to the AC terminals through the inductance L_f and its intrinsic resistance R_f.

Different configurations of static power processing units can be used as SM. The main types are the half-bridge, full-bridge, flying-capacitor, cascade half-bridge and double-clamped (DU *et al.*, 2018). However, this work focuses on the half-bridge topology for the SMs of the MMC-STATCOM due to its simplicity and low number of switches. The SM based on the half-bridge converter consists of two IGBTs and a DC capacitor with a series equivalent resistance R_C, as shown in Diagram 2. Moreover, it is considered that the parameters of all SMs of the MMC-STATCOM are equal.

Diagram 2 – Topology of the three-phase three-wire MMC-STATCOM connected to the electric network.



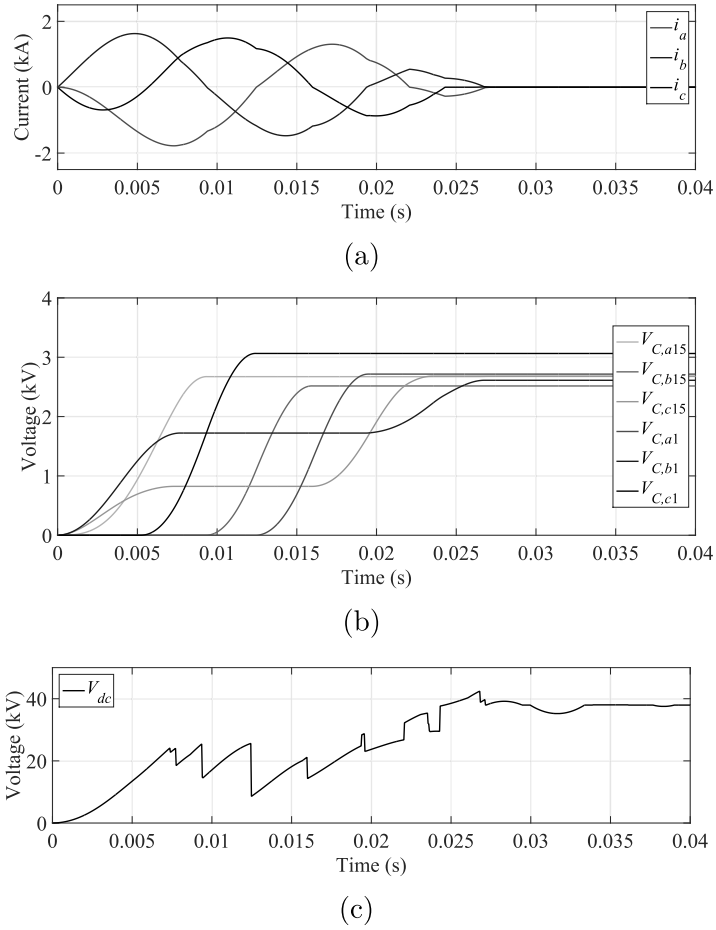
Source: Elaborated by the author (2021).

2.3 DIRECT CONNECTION OF THE MMC-STATCOM TO THE ELECTRIC NETWORK

Initially, in order only to demonstrate the need for an energizing strategy for the MMC-STATCOM, a simulation was performed in which the static compensator of Diagram 2 was directly connected to the grid with all its DC capacitors discharged. During this procedure, all IGBTs of the converter's SMs were kept open. The parameters of the electric network and MMC-STATCOM are given in Table 8 and Table 9 (Appendix A), respectively, considering 100 MVA as base power.

Figures 2 (a), (b) and (c) show the waveforms of the AC terminal line currents, the SM voltages of the lower and upper arms and the DC terminal voltage, respectively, during the MMC-STATCOM energization. It can be noted in Figure 2 (a) that the currents reach high amplitudes, of the order of kiloampers, which can damage the multilevel converter. Due to this current level the submodule DC voltages increase very fast, as shown in Figure 2 (b). Figure 2 (c) shows that the DC terminal voltage reach the peak value of the grid line-to-line voltage in less than 30 ms.

Figure 2 – Waveforms of the direct connection of the MMC-STATCOM to the electric network.



Caption: (a) AC terminal line currents, (b) DC voltages of the SMs and (c) DC terminal voltage.

Source: Elaborated by the author (2021).

In the following sections, equivalent circuits, mathematical models and the description of each stage of the energizing process proposed for the MMC-STATCOM will be presented.

2.4 THE PROPOSED ENERGIZING STRATEGY

This section presents the stages of the energizing strategy proposed for the MMC-STATCOM. Each stage is also mathematically modelled to derive control laws in order to charge all submodule DC capacitors of the static compensator.

Diagram 3 shows the MMC-STATCOM connected to the electric network through the proposed energizing circuit. This circuit is formed by a controller and two thyristors (T_1 and T_2) parallel-connected with the contacts of phases "a" and "b" of the mechanical switch used to connect the MMC-STATCOM to the grid. This topology for the energizing circuit was chosen so that the component count is low. However, other topologies can also be used for the energizing circuit. For instance, if two thyristors are connected in anti-parallel with T_1 and T_2 of Diagram 3, the energizing current is symmetric, despite the number of switches be increased. It can also be cited that the topology of the energizing circuit presented in this thesis can be used/adapted to energize other static converters.

The main advantage of the use of thyristors to energize the MMC-STATCOM is that they can be fired in such a way to control the maximum value of the energizing current during all the procedure to charge the DC capacitors of the SMs. One could think of using IGBTs instead of thyristors. However, besides the thyristors being more robust than IGBTs, the series connection of IGBTs is more complex than thyristors.

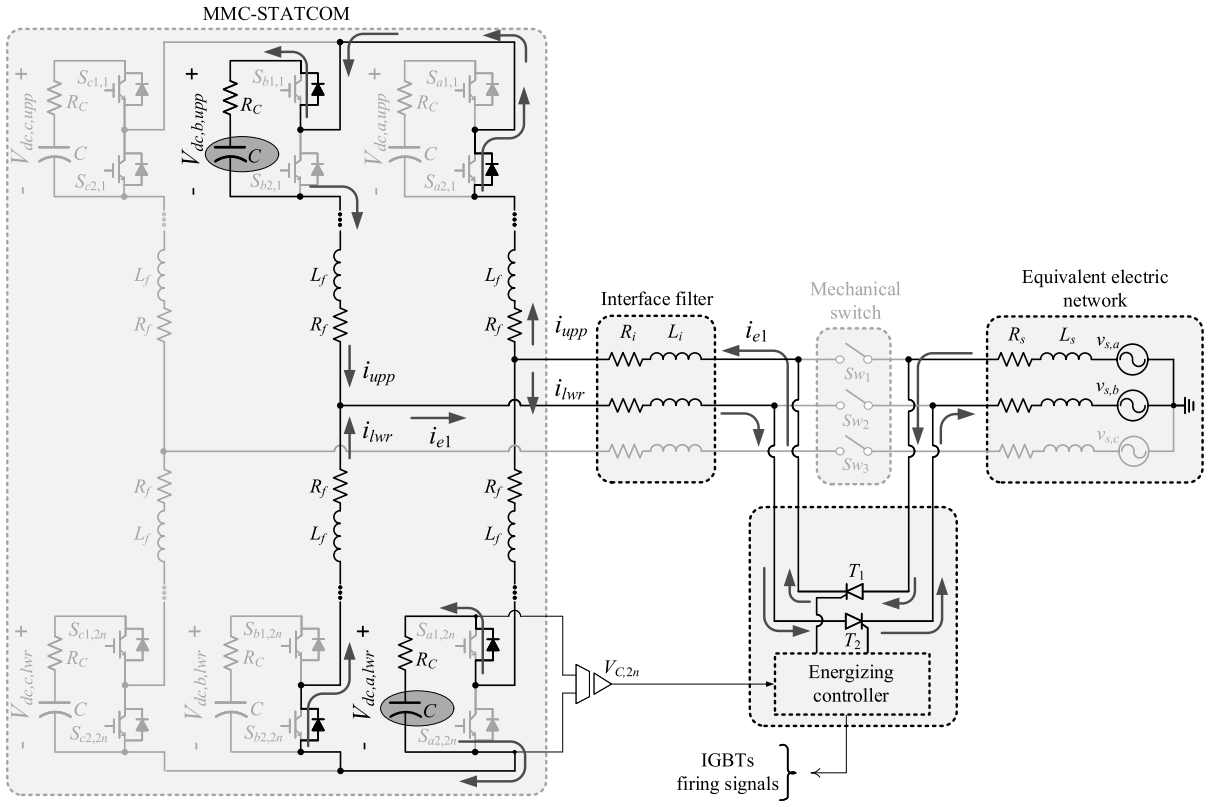
In Diagram 3, the discharge resistor of the SMs was neglected, since it has a value typically high. During the MMC-STATCOM energizing procedure, the three-phase mechanical switch is kept open. The voltage $V_{C,2n}$ across the SM $2n$ of phase "a" of the static compensator is measured and the signal is sent to the energizing controller, whose output signals are used to fire the thyristors and converter's IGBTs. The energizing process is synchronized with the grid voltage and it is divided into four stages. At the first stage, the thyristors are fired in a manner to control the current drained from the mains by the DC capacitors of the MMC-STATCOM. In the following three stages, specific IGBTs of the converter are switched to allow that the submodule DC capacitors can exchange energy, while the thyristors are kept blocked. All the energizing stages are sequentially repeated until the DC voltages of the MMC-STATCOM's arms reach the peak value of the grid line-to-line voltage. From this moment on, the mechanical switch is closed and the converter is ready to compensate for reactive power at its AC terminals.

2.4.1 **The first energizing stage**

The first energizing stage of the MMC-STATCOM starts firing the thyristors T_1 and T_2 during the positive half-cycle of the grid line-to-line voltage, in witch the derivative is negative. All IGBTs of the MMC-STATCOM are kept open during this stage.

Diagram 3 shows the direction of the current flows through the MMC-STATCOM's

Diagram 3 – Topology of the MMC-STATCOM energizing circuit.



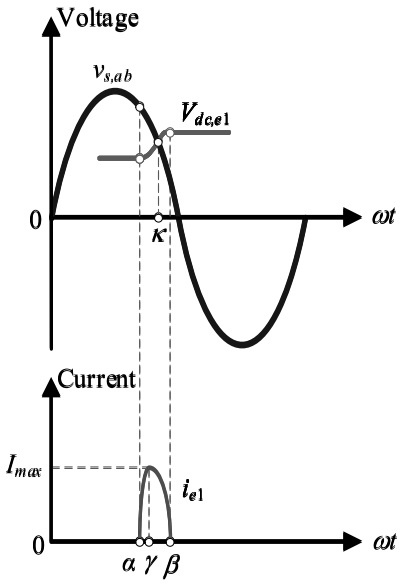
Source: Reproduced from (DUARTE; ALMEIDA; BARBOSA, 2019).

arms. All shaded elements in this figure are inactive. Considering that the capacitors of phases "a" and "b" of the lower and upper arms, respectively, are the less charged, the current drained from the grid flows through the elements shown in Diagram 3 charging the highlighted capacitors. i_{e1}, i_{upp} and $i_{\ell wr}$ are, respectively, the current drained from the grid and that flows through the upper and lower arms of phases "b" and "a", respectively. The subscript "$_{e1}$" is used to identify the first energizing stage.

Figures 3 (a) and (b) depicts the waveforms of the grid line-to-line voltage $v_{s,ab}$, the DC voltages of the MMC's arms $V_{dc,e1}$ and the energizing current i_{e1}. These figures were drawn using a generic firing angle α. The current drained from the grid reaches its maximum value when $\omega t = \gamma$. On the other hand, for $\omega t = \beta$ the current is null and the thyristors are blocked. The maximum value (I_{max}) of the current i_{e1} is controlled by firing T_1 and T_2 with an angle α smaller than κ, being κ the angle in which $v_{s,ab}$ is equal to $V_{dc,e1}$ (see Figure 3 (a)).

The maximum value of i_{e1} is directly related to the difference between the angles α and κ. The smaller the aforementioned difference the smaller the difference between the voltages $v_{s,ab}$ and $V_{dc,e1}$. Consequently, the value of I_{max} will be also smaller.

Figure 3 – Waveforms of the first energizing stage.



Caption: (a) AC and DC voltages and (b) energizing current.

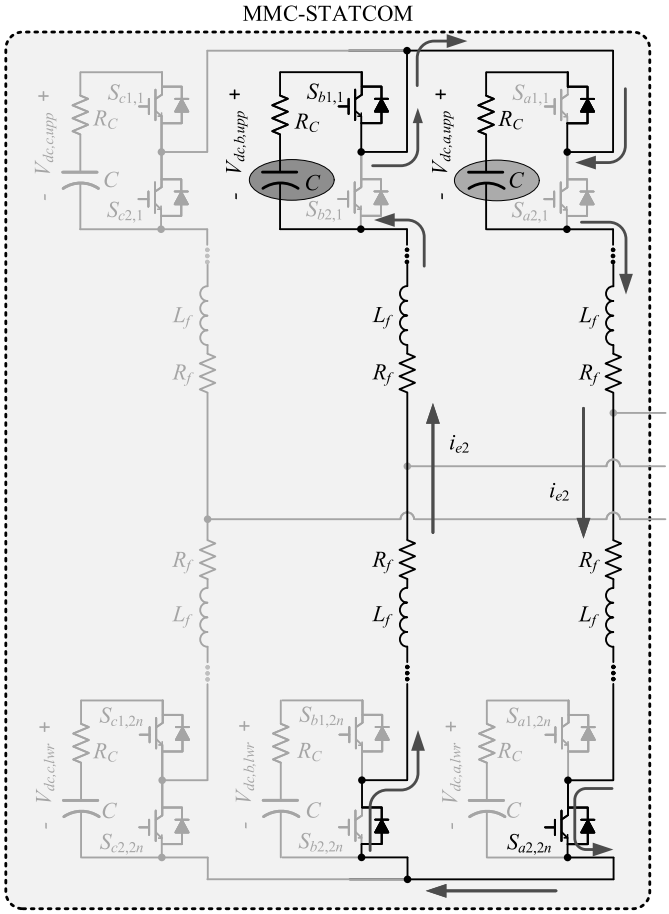
Source: Reproduced from (DUARTE; ALMEIDA; BARBOSA, 2019).

2.4.2 **The second energizing stage**

In this stage, part of the energy stored in the upper arm capacitors of phase "b", during the first stage, is transferred to the upper arm capacitors of phase "a". The thyristors T_1 and T_2 are kept open in order to maintain the MMC-STATCOM disconnected from the grid, while the upper IGBTs ($S_{b1,1}$–$S_{b1,n}$) and the lower IGBTs ($S_{a2,n+1}$–$S_{a2,2n}$) must be closed. Diagram 4 shows the topology of the equivalent circuit indicating the current flow direction between the phases "a" and "b" of the MMC-STATCOM. The current i_{e2} is responsible by the energy exchange between the DC capacitors during the second energizing stage. The capacitors highlighted in red and blue indicate the ones that are discharged and charged, respectively.

In order to ensure the correct operation of this stage, the upper and lower IGBTs of the upper and lower arms SMs of phases "a" and "b", respectively, should be kept open. This type of switching of the IGBTs differs from the complementary switching pattern used during the converter operation. However, this processes ensures that the energy is not indefinitely exchanged between the capacitors and inductors of the circuit, since the diodes do not allow a bidirectional current flow. At the and of this stage, the upper arm capacitors of phase "a" present a higher voltage level than the upper arm capacitors of phase "b".

Diagram 4 – Active switches and current flow through the MMC-STATCOM submodules during the second energizing stage.



Source: Reproduced from (DUARTE; ALMEIDA; BARBOSA, 2019).

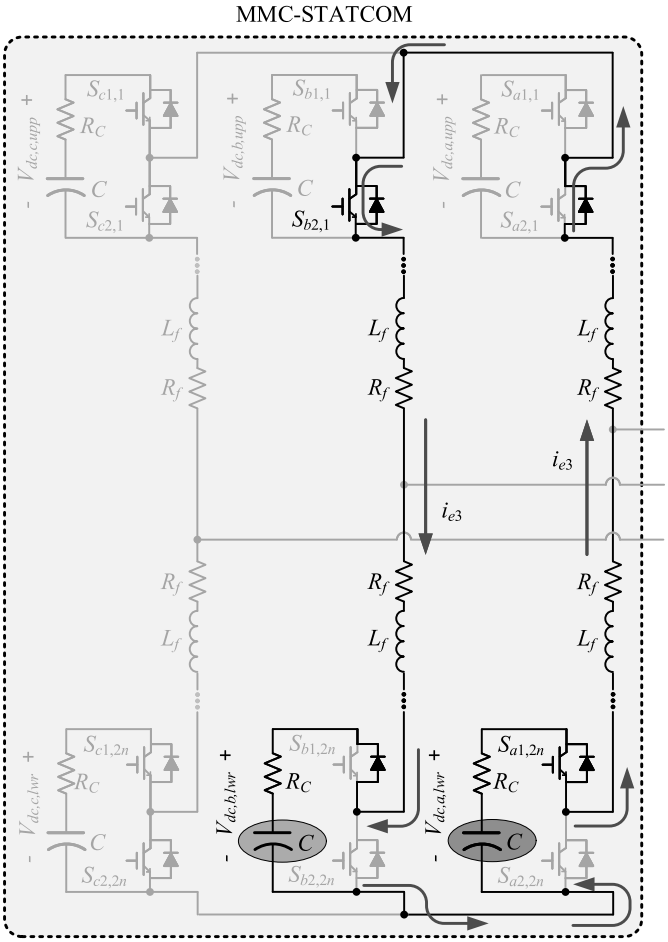
2.4.3 **The third energizing stage**

The third energizing stage is similar to the second stage. The difference is that the lower arm capacitors of phase "b" are charged by the lower arm capacitors of phase "a". During this stage, the upper IGBTs ($S_{a1,n+1}$–$S_{a1,2n}$) and the lower IGBTs ($S_{b2,1}$–$S_{b2,n}$) are kept closed. Diagram 5 shows the topology of the equivalent circuit indicating the current flow direction between the SMs of phases "a" and "b". The current i_{e3} is responsible by the energy exchange between the DC capacitors during the third energizing stage. In a manner similar to the previous stage, All IGBTs of the upper and lower arms of phases "a" and "b", respectively, should be kept open. At the and of this stage, the lower arm capacitors of phase "a" present a voltage lower than the lower arm capacitors of phase "b".

2.4.4 **The fourth energizing stage**

Finally, in the fourth stage, the upper and lower arm capacitors of phase "c" are charged using the energy stored in the capacitors of phases "a" and "b". Diagram 6 shows

Diagram 5 – Active switches and current flow through the MMC-STATCOM submodules during the third energizing stage.



Source: Reproduced from (DUARTE; ALMEIDA; BARBOSA, 2019).

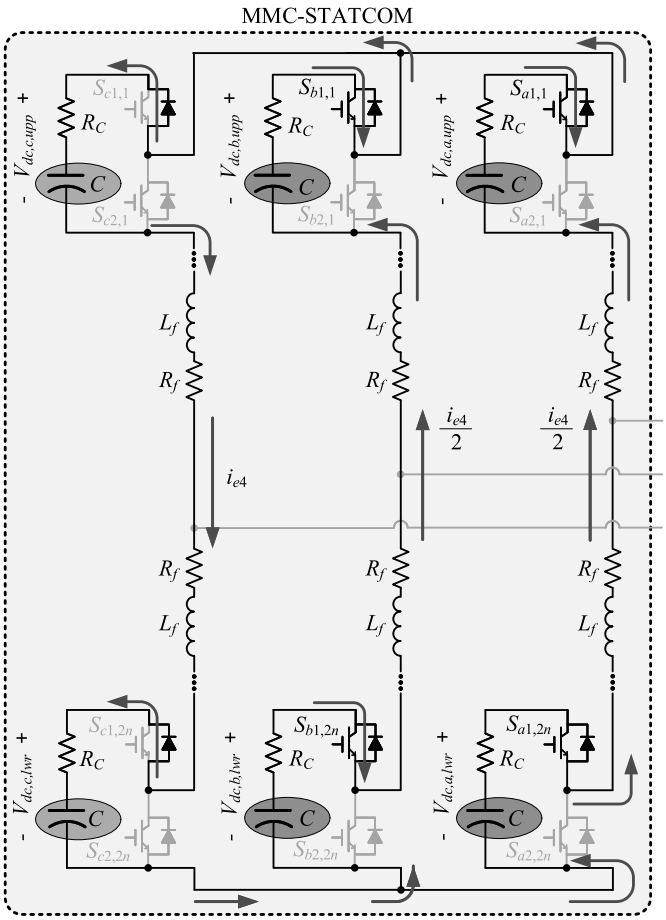
the equivalent circuit topology of the fourth stage indicating the current flows through the converter's SMs. The current i_{e4} is responsible by the energy exchange between the capacitors during the fourth stage. All upper IGBTs of the SMs of phase "a" ($S_{a1,1}$–$S_{a1,2n}$) and phase "b" ($S_{b1,1}$–$S_{b1,2n}$) are kept closed, while the upper and lower IGBTs of the SMs of phase "c" are kept open.

Although the voltages of the upper and lower arm capacitors of phase "a" are different from the voltages of the upper and lower arm capacitors of phase "b", the sum of all DC voltages in each phase is the same. Again, the capacitors highlighted in red and blue indicate the ones that are discharged and charged, respectively.

At the end of this stage, the lower and upper arm capacitors of phases "a" and "b", respectively, have less stored energy than the capacitors of the same leg. At first sight, this condition may seen a problem. However, this will ensure that only the mentioned capacitors, with less energy, will be charged when the thyristors T_1 and T_2 are fired in the

next positive semi-cycle of the grid voltage.

Diagram 6 – Active switches and current flow through the MMC-STATCOM submodules during the fourth energizing stage.



Source: Reproduced from (DUARTE; ALMEIDA; BARBOSA, 2019).

2.5 MATHEMATICAL MODELLING OF THE PROPOSED ENERGIZING PROCESS

The energizing stages previously described are repeated until the DC voltages of the MMC-STATCOM's arms reach the peak value of the grid line-to-line voltage. In this section, the equivalent circuits of each energizing stage are mathematically modelled in order to obtain a control law to regulate the energizing current of the MMC-STATCOM.

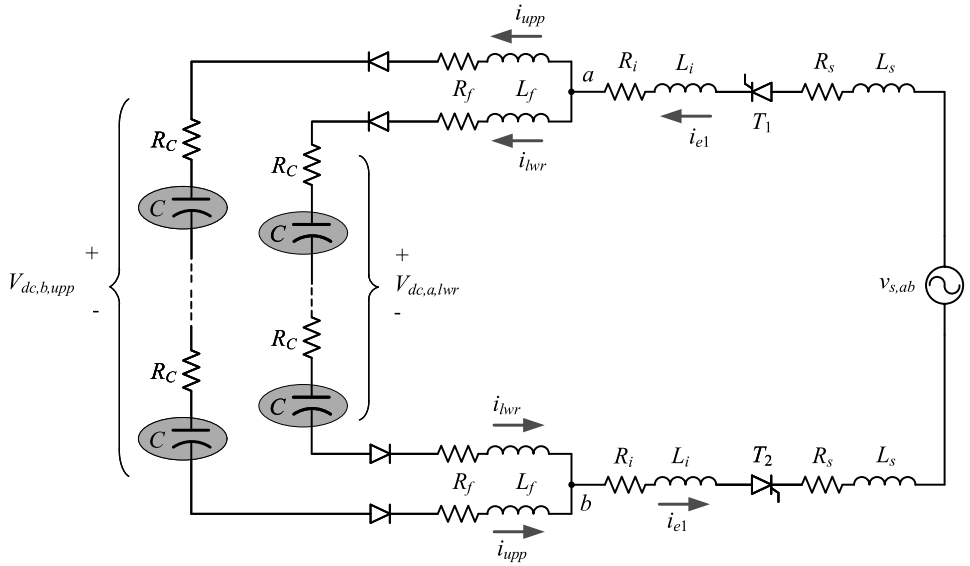
Although this work focuses on the half-bridge topology for the SMs, the thyristors can also be used to control the energizing current of a MMC-STATCOM with other SM topologies, such as the full-bridge converter. However each energizing stage must be designed for each SM topology in a case-by-case analysis, since different SMs provide different path for the energizing current.

2.5.1 **Capacitors charging during the first energizing stage**

As the DC capacitor voltages start increasing due to the energizing process, the thyristors firing angle should be reduced every cycle of the energizing process to ensure that the energizing current is drained from the grid.

Having in mind the circuit shown in Diagram 3 it is possible to drawn the equivalent circuit of Diagram 7. Assuming that the thyristors T_1 and T_2 are fired at $\omega t = \alpha$ (see Figure 3), the following system of differential equations can be written for the equivalent circuit composed by the lower and upper arm SMs of phases "a" and "b", respectively:

Diagram 7 – Equivalent circuit for the first energizing stage.



Source: Reproduced from (DUARTE; ALMEIDA; BARBOSA, 2019).

$$
\begin{cases}
2L_f \dfrac{di_{\ell wr}(t)}{dt} + \dfrac{n}{C}\displaystyle\int_0^t i_{\ell wr}(\lambda)d\lambda + R_t i_{\ell wr}(t) + 2L_{eq}\dfrac{di_{e1}(t)}{dt} + 2R_{eq}i_{e1}(t) = \\
= \left[v_{s,ab}(t) - V_{dc,a,\ell wr}\left(t_\alpha^-\right)\right]\ u_{-1}\left(t - t_\alpha\right) \\
\\
2L_f \dfrac{di_{upp}(t)}{dt} + \dfrac{n}{C}\displaystyle\int_0^t i_{upp}(\lambda)d\lambda + R_t i_{upp}(t) = 2L_f \dfrac{di_{\ell wr}(t)}{dt} + \dfrac{n}{C}\displaystyle\int_0^t i_{\ell wr}(\lambda)d\lambda + R_t i_{\ell wr}(t) + \\
+ \left[V_{dc,a,\ell wr}\left(t_\alpha^-\right) - V_{dc,b,upp}\left(t_\alpha^-\right)\right]\ u_{-1}\left(t - t_\alpha\right) \\
\\
i_{e1}(t) = i_{\ell wr}(t) + i_{upp}(t)
\end{cases}
\tag{2.1}
$$

where $L_{eq} = (L_s + L_i)$ is the equivalent inductance and $R_{eq} = (R_s + R_i)$ is the equivalent resistance, both seen from the MMC AC terminals; $R_t = (2R_f + 2nR_D + nR_C)$ is the equivalent resistance of the converter seen from the input terminals of the interface filter; n is the number of SMs per arm of the MMC-STATCOM and R_D is the diodes

conduction resistance of the IGBTs; $V_{dc,a,\ell wr}$ is the sum of the lower arm capacitor voltages of phase "a"; $V_{dc,b,upp}$ is the sum of the upper arm capacitor voltages of phase "b"; $v_{s,ab}(t) = \sqrt{2}V_L \sin(\omega_s t)$ is the grid line-to-line voltage and $u_{-1}(t - t_\alpha)$ is the unitary step function applied at t_α; $t_\alpha^- = (\alpha^-/\omega_s)$ and $t_\alpha = (\alpha/\omega_s)$ are the instants immediately before and after the thyristor firing pulses, respectively; $\omega_s = 2\pi f_s$ is the fundamental angular frequency and f_s is the fundamental frequency of the electric network.

Applying the Laplace transform in (2.1), considering the following initial conditions:

$$\begin{cases} i_{e1}(\alpha^-/\omega_s) = 0 \\ i_{upp}(\alpha^-/\omega_s) = 0 \\ i_{\ell wr}(\alpha^-/\omega_s) = 0 \\ V_{dc,b,upp}(\alpha^-/\omega_s) = V_{dc,b,upp} \\ V_{dc,a,\ell wr}(\alpha^-/\omega_s) = V_{dc,a,\ell wr} \end{cases}, \tag{2.2}$$

the following expressions are obtained in the frequency domain:

$$\begin{cases} \sqrt{2}V_L e^{-st_\alpha}\left[\dfrac{s\ \sin(\alpha) + \omega_s\ \cos(\alpha)}{(s^2+\omega_s^2)(s^2+2\zeta s+\omega_r^2)}\right] = R_t I_{\ell wr}(s) + \\ +2sL_f I_{\ell wr}(s) + \dfrac{n}{sC} I_{\ell wr}(s) + \dfrac{V_{dc,a,\ell wr}\ e^{-st_\alpha}}{s} + 2sL_{eq} I_{e1}(s) + 2R_{eq} I_{e1}(s) \\ \\ 2sL_f I_{\ell wr}(s) + \dfrac{n}{sC} I_{\ell wr}(s) + R_t I_{\ell wr}(s) + \dfrac{V_{dc,a,\ell wr}\ e^{-st_\alpha}}{s} = \\ = 2sL_f I_{upp}(s) + \dfrac{n}{sC} I_{upp}(s) + R_t I_{upp}(s) + \dfrac{V_{dc,b,upp}\ e^{-st_\alpha}}{s} \\ \\ I_{e1}(s) = I_{upp}(s) + I_{\ell wr}(s) \end{cases}. \tag{2.3}$$

Solving (2.3) for $I_{e1}(s)$, considering $V_{dc,e1} = V_{dc,b,upp} = V_{dc,a,\ell wr}$, the energizing current drained from the grid, in the time domain, is given by:

$$I_{e1}(s) = \left(\frac{\sqrt{2}V_L}{L_{eq,e1}}\right)\frac{e^{-st_\alpha} s\,(\omega_s\ \cos\alpha + s\ \sin\alpha)}{(s^2+\omega_s^2)(s^2+2\zeta s+\omega_r^2)} - \left(\frac{V_{dc,e1}}{L_{eq,e1}}\right)\frac{e^{-st_\alpha}}{s^2+2\zeta s+\omega_r^2}, \tag{2.4}$$

where $\zeta = R_{eq,e1}/(2L_{eq,e1})$ is the damping factor and $\omega_r = \sqrt{n/(2C_{eq,e1}L_{eq,e1})}$ is the resonant frequency of the equivalent circuit for the first energizing stage; $L_{eq,e1} = (2L_{eq} + L_f)$, $R_{eq,e1} = (2R_{eq} + R_t/2)$ and $C_{eq,e1} = 2C/n$. The subscript $_{e1}$ was included to the previous variables to make reference to the first energizing stage.

Applying the inverse Laplace transform in (2.4), the energizing current of the MMC-STATCOM, in the time domain, is given by the following expression:

$$
\begin{aligned}
i_{e1}(t) = \tfrac{\sqrt{2}(V_L/L_{eq,e1})}{(2\zeta\omega_s)^2+(\omega_s^2-\omega_r^2)^2}\Big\{ & 2\zeta\omega_s^2\sin(\omega_s t) + \omega_s\left(\omega_r^2-\omega_s^2\right)\cos(\omega_s t) - \\
-\Big[\zeta\omega_s^2 e^{(\omega_d-\zeta)(t-t_\alpha)} + \zeta\omega_s^2 e^{-(\omega_d+\zeta)(t-t_\alpha)} + \left(\tfrac{2\zeta^2\omega_s^2-\omega_s^2\omega_r^2+\omega_r^4}{2\omega_d}\right)e^{-(\omega_d+\zeta)(t-t_\alpha)} - \\
-\left(\tfrac{2\zeta^2\omega_s^2-\omega_s^2\omega_r^2+\omega_r^4}{2\omega_d}\right)e^{(\omega_d-\zeta)(t-t_\alpha)}\Big]\sin(\alpha) - \omega_s e^{-\zeta(t-t_\alpha)}\Big[\left(\omega_r^2-\omega_s^2\right)\cosh\left[\omega_d\left(t-t_\alpha\right)\right] + \\
+\tfrac{\zeta\left(\omega_r^2+\omega_s^2\right)}{\omega_d}\sinh\left[\omega_d\left(t-t_\alpha\right)\right]\Big]\cos(\alpha)\Big\}u_{-1}\left(t-t_\alpha\right) + \\
+\left(\tfrac{V_{dc,e1}}{2\omega_d L_{eq,e1}}\right)\left[e^{-(\omega_d+\zeta)(t-t_\alpha)} - e^{(\omega_d-\zeta)(t-t_\alpha)}\right]u_{-1}\left(t-t_\alpha\right), \qquad (2.5)
\end{aligned}
$$

where $\omega_d = \sqrt{\zeta^2 - \omega_r^2}$.

The expression (2.5) is valid only for $\alpha \leq \omega_s t \leq \beta$. In the next section, this expression will be used to limit the maximum value of the current i_{e1} drained from the grid.

2.5.2 Control of the energizing current

Considering that there are no currents flowing through the SMs of the MMC-STATCOM at t_α^-, the following relation can be written:

$$
V_{dc,e1} = n(V_{C,2n}), \qquad (2.6)
$$

where $V_{C,2n}$ is the DC voltage of the SM capacitor $2n$ of phase "a".

Substituting (2.6) in (2.5), the following system of equations can be written:

$$
\begin{cases} i_{e1}(t_\gamma, \alpha) = I_{max} \\ \dfrac{\partial i_{e1}(t_\gamma, \alpha)}{\partial t_\gamma} = 0 \end{cases}, \qquad (2.7)
$$

where I_{max} is the maximum value desired for the current i_{e1}, which depends on the angle α and the time t_γ, being $t_\gamma = (\gamma/\omega_s)$ the time this value occurs.

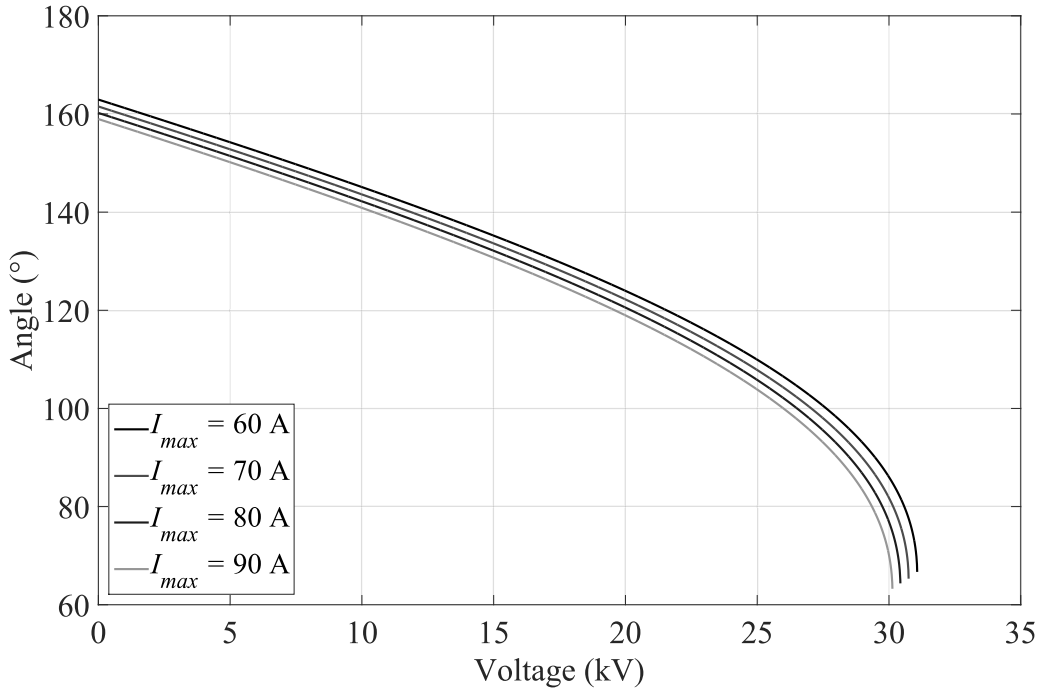
The non-linear system represented by (2.7) can be numerically solved using the Newton-Raphson method, as shown below:

$$
\begin{bmatrix} \Delta\alpha \\ \Delta t_\gamma \end{bmatrix} = \begin{bmatrix} \dfrac{\partial i_{e1}}{\partial t_\gamma} & \dfrac{\partial i_{e1}}{\partial \alpha} \\ \dfrac{\partial^2 i_{e1}}{\partial t_\gamma^2} & \dfrac{\partial^2 i_{e1}}{\partial \alpha \partial t_\gamma} \end{bmatrix}^{-1} \begin{bmatrix} (I_{max} - i_{e1}) \\ 0 - \dfrac{\partial i_{e1}}{\partial t_\gamma} \end{bmatrix}, \qquad (2.8)
$$

where $\Delta\alpha$ and Δt_γ are the mismatches of α and t_γ, respectively.

Figure 4 shows the energizing characteristic curves (α x V_{dc}), obtained by solving (2.8), for different values of I_{max}, where the DC voltage was varied with an increment of 1 V. The parameters of the electric network and MMC-STATCOM are the same of those shown in Tables 8 and 9, respectively. The lower the value of I_{max} the lower the voltage drops across the circuit's resistances and inductances. It can be noted in Figure 4 that this condition allows the DC voltages of the MMC's arms reach values close to the peak value of the grid line-to-line voltage. Thus, this energizing characteristic curve gives the firing angle of the thyristors, for each measured DC voltage, so that the peak value of the energizing current is I_{max}.

Figure 4 – Characteristic curves α x V_{dc} for the first energizing stage.



Source: Elaborated by the author (2021).

Besides the angles α it is also necessary to compute the angles β in which the energizing current become null and the thyristors are blocked (see Figure 3). Thus, in the next section these angles will be calculated in order to obtain the time period of the first energizing stage.

2.5.3 **The time period of the first energizing stage**

Substituting the values of α and V_{dc} (calculated in the Subection 2.5.2) in (2.5), the angle β is calculated by:

$$i_{e1}(t_\beta, \alpha) = 0, \tag{2.9}$$

where $t_\beta = (\beta/\omega_s)$ is the instant the current i_{e1} is null (see Figure 3).

Using the Newton-Raphson method, (2.9) is solved by:

$$\Delta t_\beta = \left[\frac{\partial i(t_\beta, \alpha)}{\partial t_\beta}\right]^{-1} \left[0 - i(t_\beta, \alpha)\right], \tag{2.10}$$

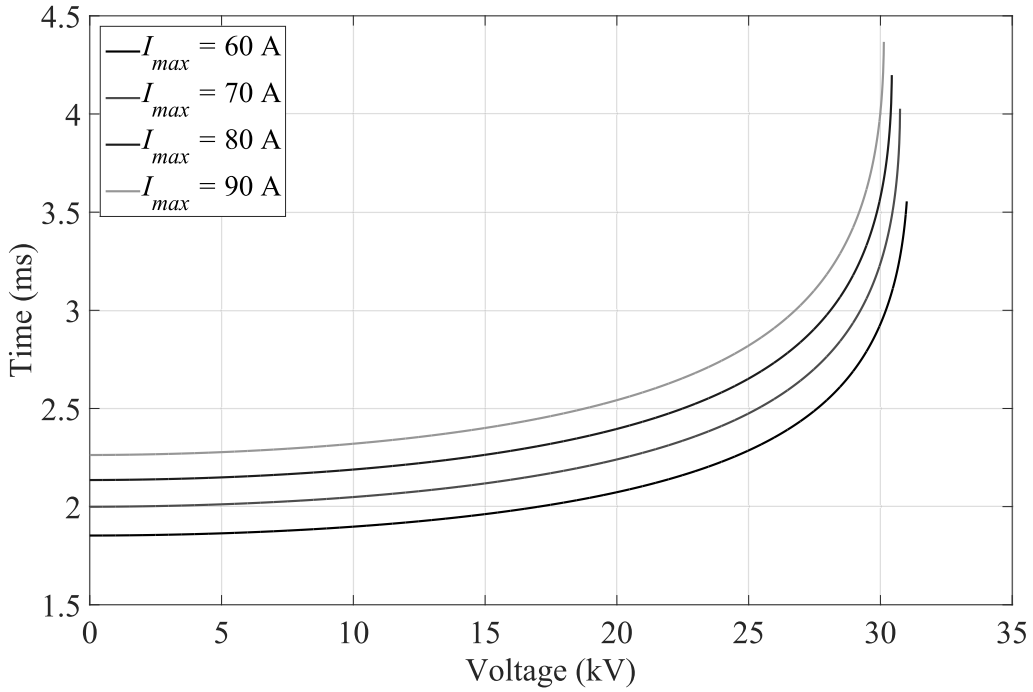
where Δt_β is the mismatch of t_β.

Since the angles α and β were computed, the time period of the first energizing stage can be calculated by:

$$T_{e1} = \frac{\beta - \alpha}{\omega_s} = t_\beta - t_\alpha. \tag{2.11}$$

Figure 5 shows the characteristic curve of the energizing time periods as a function of the DC voltage, for each value of I_{max}. It can be noted that the higher the value of I_{max} the higher the time periods of the first stage. Moreover, as the DC capacitors of the MMC-STATCOM are charged the energizing time periods increase. This occurs due to the lower difference between the DC capacitors and grid voltages. Since the maximum value of the current i_{e1} is limited to I_{max}, the energizing time periods also increase.

Figure 5 – Characteristic curves for the time periods of the first energizing stage.



Source: Elaborated by the author (2021).

This time period and the time periods of the following energizing stages (presented in the next sections) will be used to define the longest period of time, among the four

energizing stages, used to design the energizing controller of the MMC-STATCOM. For the first energizing stage, the higher time period of the curve chosen in Figure 5 should be taken into account.

Besides impacting the energizing time period the value of I_{max} should be chosen in order to minimize the impacts on the electrical network caused by the energizing current during the first stage, since the asymmetric current flow through the grid can cause power losses, transformer saturation and damage to electric motors (HART, 2011). Thus, in the next section the DC energizing current will be mathematically modelled.

2.5.4 DC energizing current

From Figure 3, the average value of the energizing current can be calculated by:

$$\bar{I}_{e1} = \left(\frac{1}{T_s}\right) \int_{t_\alpha}^{t_\beta} i_{e1}(t)dt, \tag{2.12}$$

where $T_s = 2\pi/\omega_s$ is the period of the grid voltage.

Substituting (2.5) in (2.12) the following expression is obtained for the average energizing current:

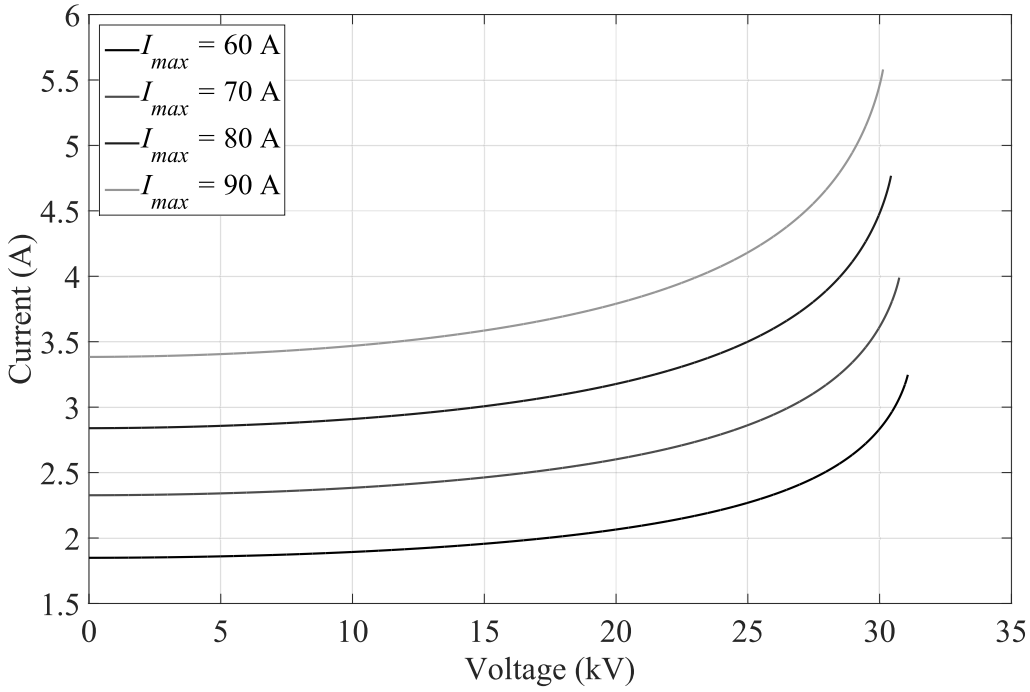
$$\begin{aligned}
\bar{I}_{e1} = {} & \frac{\sqrt{2}V_L u_{-1}\left(t_\beta - t_\alpha\right)}{2L_{eq,e1}T_s\left[\left(2\zeta\omega_s\right)^2 + \left(\omega_s^2 - \omega_r^2\right)\right]} \left\{2\left(\omega_r^2 - \omega_s^2\right)\sin\left(\beta\right) - 4\zeta\omega_s\cos\left(\beta\right) + \right. \\
& + e^{\left(t_\beta - t_\alpha\right)\frac{\left(\omega_d - \zeta\right)}{\omega_s}} \left\{\frac{\omega_s\cos(\alpha)}{\omega_d}\left[2\zeta\omega_d\left(1 + e^{\left(t_\alpha - t_\beta\right)\frac{2\omega_d}{\omega_s}}\right) + \left(\omega_r^2 - 2\zeta^2 - \omega_s^2\right)\left(e^{\left(t_\alpha - t_\beta\right)\frac{2\omega_d}{\omega_s}} - 1\right)\right] - \right. \\
& \left. \left. - \sin(\alpha)\left[\left(\omega_r^2 - \omega_s^2\right)\left(1 + e^{\left(t_\alpha - t_\beta\right)\frac{2\omega_d}{\omega_s}}\right) - \frac{\zeta\left(\omega_r^2 + \omega_s^2\right)}{\omega_d}\left(e^{\left(t_\alpha - t_\beta\right)\frac{2\omega_d}{\omega_s}} - 1\right)\right]\right\}\right\} + \\
& + \frac{V_{dc}u_{-1}\left(t_\beta - t_\alpha\right)}{2L_{eq,e1}T_s\omega_r^2}\left\{\left(1 + \frac{\zeta}{\omega_d}\right)e^{\left(t_\beta - t_\alpha\right)\frac{\left(\omega_d - \zeta\right)}{\omega_s}} + \left(1 - \frac{\zeta}{\omega_d}\right)e^{\left(t_\alpha - t_\beta\right)\frac{\left(\omega_d + \zeta\right)}{\omega_s}} - 2\right\}.
\end{aligned} \tag{2.13}$$

The angles α and β, calculated in the Subection 2.5.2 and Subection 2.5.3, respectively, can be substituted in (2.13) to calculate the DC energizing current of the MMC-STATCOM.

Figure 6 shows the average values of the energizing current, during the DC capacitors charging, for different values of I_{max}. The higher the value of I_{max} the higher the average value of the energizing current. Moreover, as the DC capacitors are charged the DC current becomes higher, since the energizing times shown in Figure 5 are also higher.

In addition to all the considerations already made regarding the maximum value of the energizing current (I_{max}), this value should be chosen in order to ensure the lifetime of the SM capacitors. Therefore, the value I_{max} should be chosen in order to respect the oscillating currents limits available in the DC capacitor datasheets and allowed for specific frequencies and temperatures. For instance, in a 450 V/4700 µF capacitor manufactured by EPCOS the oscillation current is 15.68 A and 9.8 A, at 120 Hz, for the temperatures

Figure 6 – Characteristic curves for the average values of the first stage energizing current.



Source: Elaborated by the author (2021).

of 40 °C and 85 °C, respectively. However, the current through each DC capacitor will depend on the number of capacitors connected in series/parallel to compose the bank of capacitors of each SM. Thus, in practice, it is necessary to perform a case-by-case analysis. Moreover, as the datasheets do not provide the limits of oscillation current for all frequencies it is important to keep low the peak value of the energizing current.

2.5.5 **Piecewise linear approximation of the control law**

The solution of (2.8) in real-time implies a great computational effort. Thus, the Piecewise Linear (PWL) approximation is used to reduce the computational burden of the energizing algorithm, since it allows the mathematical representation of non-linear curves by line segments (CHUA; LIN, 1975; DUARTE *et al.*, 2018). Considering a PWL approximation with n_q breaking points, the angle α can be calculated by:

$$\alpha_{pwl}(V_{dc}) = a + bV_{dc} + \sum_{k=1}^{n_q} c_k \left| V_{dc} - V_{dc,k} \right|, \tag{2.14}$$

where a and b are the independent and linear coefficients, respectively; $V_{dc,k}$ and c_k are the breaking points and the generic coefficients of the PWL approximation, respectively; α_{pwl} is the angle provided by the PWL approximation and k is an integer number.

The angular coefficients of the line segments between the points r and $(r+1)$ of

the PWL approximation are given by:

$$m_r = \frac{\alpha_{(r+1)} - \alpha_r}{V_{dc,(r+1)} - V_{dc,r}}, \tag{2.15}$$

where $\{r \in \mathbb{Z}_+ | 0 \leq r \leq n_q\}$.

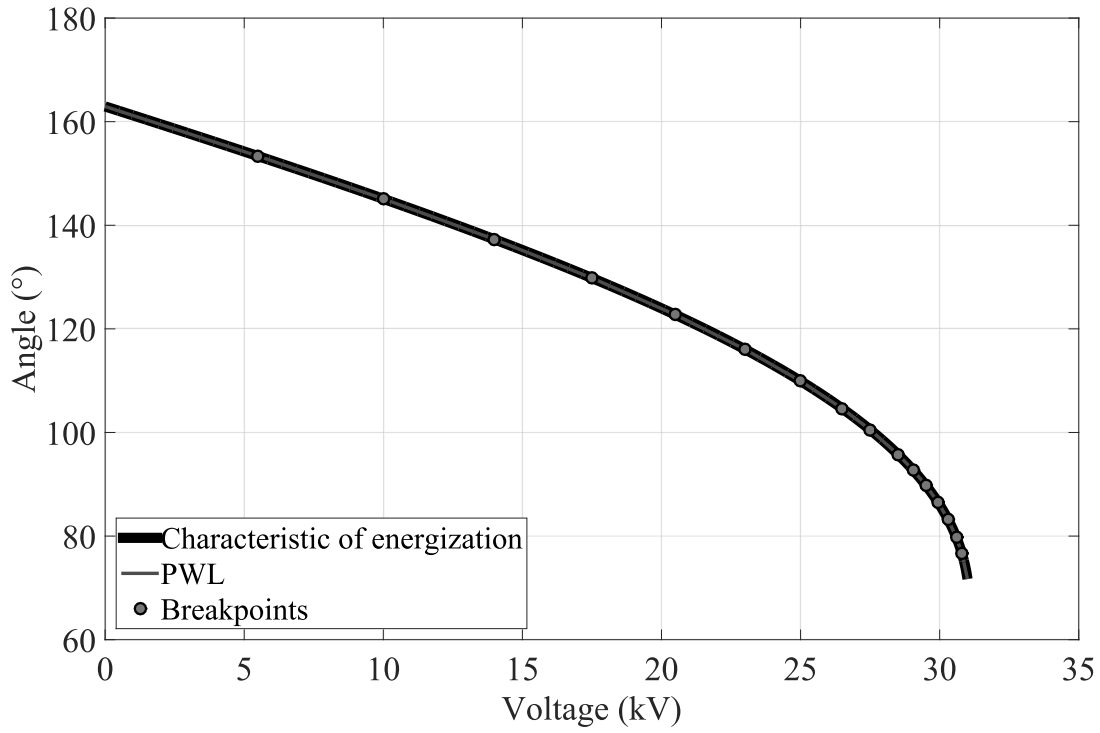
The coefficients of the PWL approximation are calculated by:

$$\begin{cases} a = \alpha_0 - \sum_{k=1}^{n_q} c_k \left| V_{dc,k} \right| \\ b = \left(\frac{m_0 + m_{n_q}}{2} \right) \\ c_k = \left(\frac{m_k - m_{(k-1)}}{2} \right) \end{cases}, \tag{2.16}$$

where α_0 is the angle for $V_{dc} = 0$ and m_0 and m_{n_q} are the extreme slopes of the PWL approximation.

Figure 7 shows the PWL approximation for the energizing characteristic ($I_{max} =$ 60 A) of Figure 4. In this case, the converter's DC capacitors are charged by the energizing current with constant peak value. Table 18 (Appendix C) shows the values of the breaking points and the coefficients a, b and c_k of the PWL approximation of Figure 7.

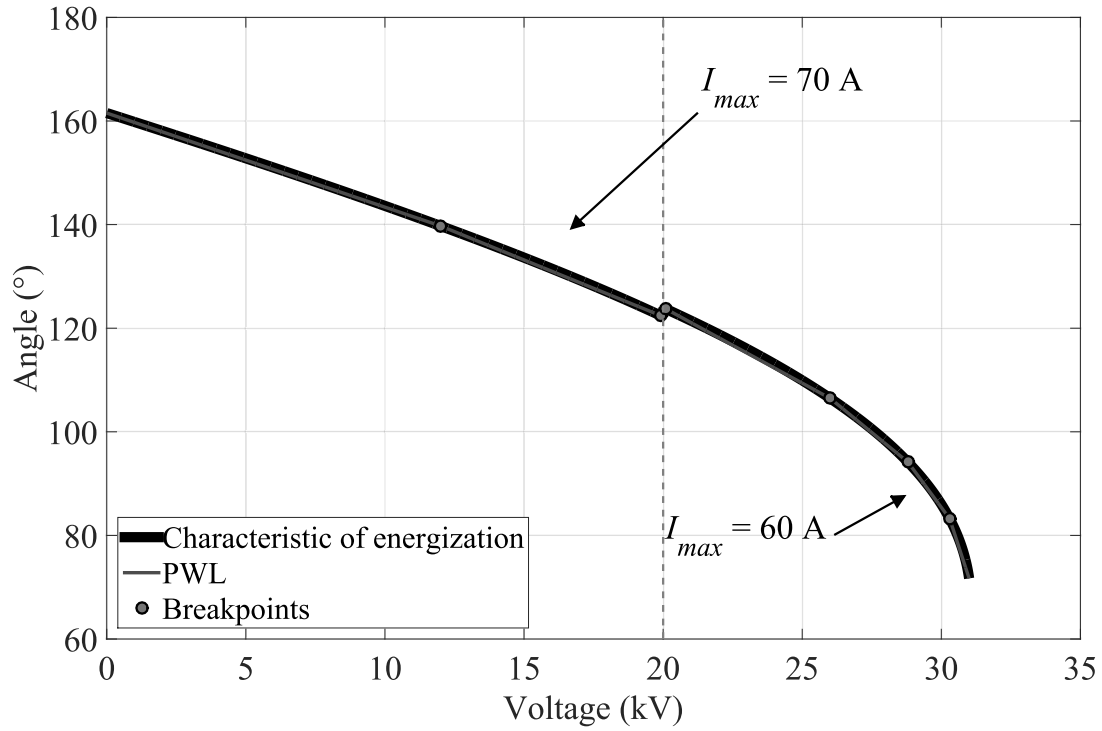
Figure 7 – Piecewise linear approximation for the energizing characteristic curve α x V_{dc} ($I_{max} = 60$ A).



Source: Elaborated by the author (2021).

Figure 8 shows the PWL approximation for two energizing characteristic curves, one for I_{max} = 70 A ($V_{dc} < 20$ kV) and another for I_{max} = 60 A ($V_{dc} \geq 20$ kV). This strategy was used to increase the DC voltages of the MMC's arms until a value close to the peak of the grid line-to-line voltage (33.94 kV). Table 19 (Appendix C) shows the values of the breaking points and the coefficients of the PWL approximation of Figure 8.

Figure 8 – Piecewise linear approximation for the energizing characteristic curves α x V_{dc} (I_{max} = 60 A and I_{max} = 70 A).



Source: Elaborated by the author (2021).

It is important to mention that the steps to obtain the expression (2.14) are not performed in real-time. Thus, after the calculation of the PWL approximation, the angle α_{pwl} is computed for each measured value of the DC voltage by only substituting V_{dc} in (2.14). Moreover, it is important to cite that experimental results of the implementation of (2.14) were shown in (DUARTE *et al.*, 2018).

2.5.6 **Energy exchange between the SM capacitors**

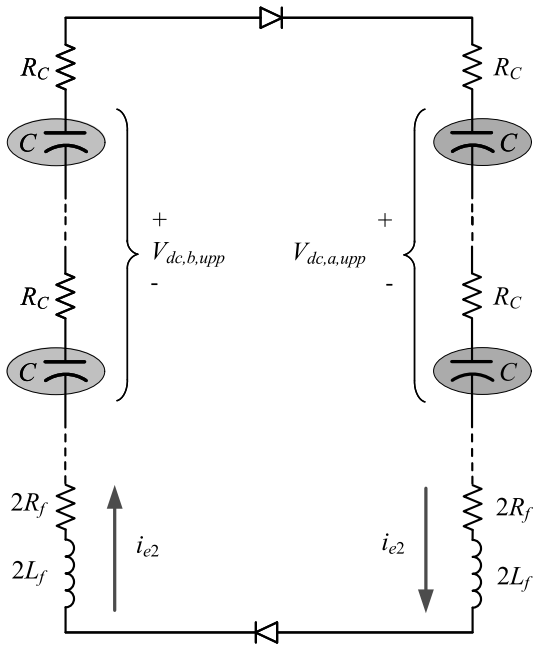
The energizing stages 2, 3 and 4 will ensure the energy exchange between the SM capacitors of the MMC-STATCOM. During these stages the thyristors T_1 and T_2 are kept blocked. Comparing the Diagram 4 and Diagram 5 it can be noted that the stages 2 and 3 present similar dynamic behaviour. Moreover, the only difference between the fourth stage and the two previous stages is the number of capacitors and inductors series-

and parallel-connected, as shown in Diagram 6. Thus, due to these similarities, only the analysis of the stages 2 and 4 will be presented in the following sections.

2.5.7 **Modelling of the second energizing stage**

Diagram 8 shows the equivalent circuit of the second energizing stage. Figure 9 (a) and Figure 9 (b) show the waveforms of the upper arm submodule DC voltages of phases "a" and "b" ($V_{dc,a,upp}$ and $V_{dc,b,upp}$) and the current through the submodule DC capacitors.

Diagram 8 – Equivalent circuit for the second energizing stage.



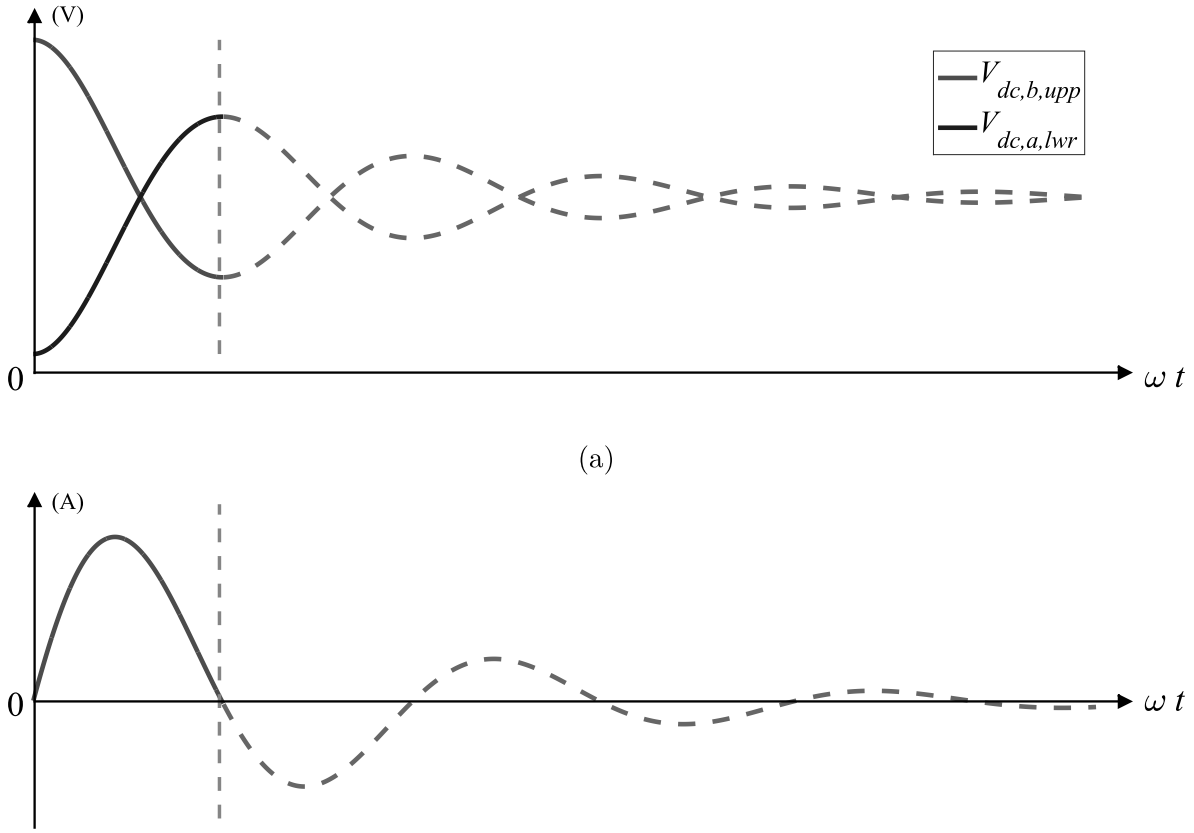
Source: Reproduced from (DUARTE; ALMEIDA; BARBOSA, 2019).

The circulating current does not become negative due to the diodes of the IGBTs. Therefore, the upper arm SM capacitors of phase "b" are only discharged while the upper arm SM capacitors of phase "a" are only charged, as shown in Figure 9 (a). When the current i_{e2} tends to become negative, the diodes of the IGBTs open the circuit. Thus, at the end of this stage, the capacitors that were charged present a voltage level higher than the ones that were discharged.

For the equivalent circuit of Diagram 8, the following differential equation can be written:

$$\left[V_{dc,b,upp}\left(t_{e2}^{-}\right) - V_{dc,a,upp}\left(t_{e2}^{-}\right)\right] u_{-1}(t - t_{e2}) = i_{e2}\left(2nR_C + R_{eq,e2}\right) + \\ + L_{eq,e2}\frac{di_{e2}}{dt} + \frac{1}{C_{eq,e2}}\int_0^t i_{e2}\left(\lambda\right) d\lambda, \tag{2.17}$$

Figure 9 – Waveforms of the second energizing stage.



Caption: (a) upper and lower arm submodule DC voltages and (b) current through the circuit.

Source: Reproduced from (DUARTE; ALMEIDA; BARBOSA, 2019).

where $R_{eq,e2} = (4R_f + 2nR_{igbt} + 2nR_D)$, $L_{eq,e2} = 4L_f$ and $C_{eq,e2} = C/2n$ are the equivalent resistance, inductance and capacitance of the second energizing stage, respectively; and t_{e2} is the time the second stage starts.

The oscillation frequency of the waveforms shown in Figure 9 can be easily calculated by applying the Laplace transform in (2.17), as follows:

$$\frac{\left[V_{dc,b,upp}\left(t_{e2}^{-}\right) - V_{dc,a,upp}\left(t_{e2}^{-}\right)\right] e^{-st_{e2}}}{L_{eq,e2}} = I_{e2}(s)\left(s^2 + 2s\zeta_{e2} + \omega_{e2}^2\right), \tag{2.18}$$

where $\omega_{e2} = 1/\sqrt{L_{eq,e2}C_{eq,e2}}$ is the natural oscillation frequency and $\zeta_{e2} = (R_{eq,e2} + 2nR_C)/(2L_{eq,e2})$ is the damping factor.

Since the frequency ω_{e2} is calculated, the period of time in which the energy

exchange among the capacitors involved in this stage occurs is given by:

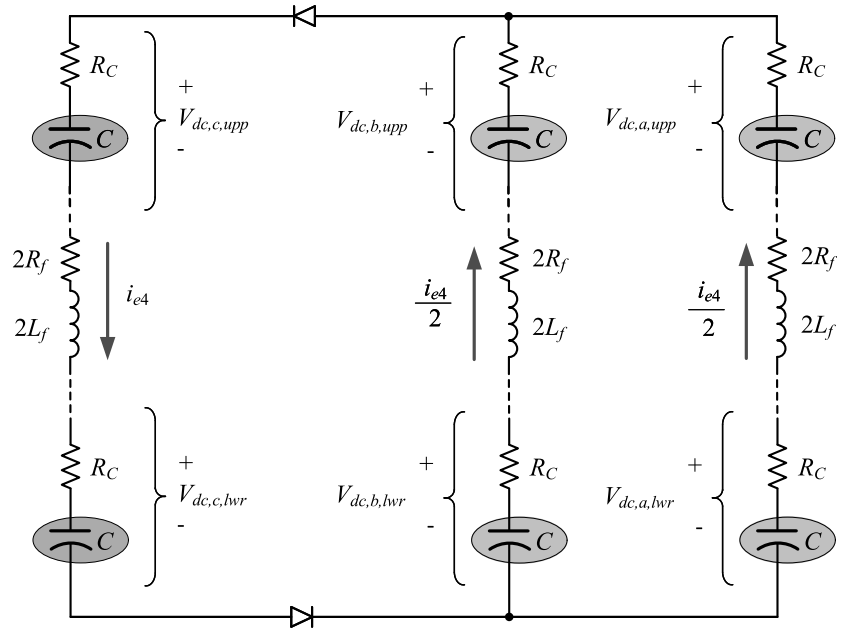
$$T_{e2} = \frac{1}{2}\left(\frac{2\pi}{\omega_{e2}}\right). \tag{2.19}$$

The value of T_{e2} is the minimum time period the circuit should be kept in the second energizing stage in order to ensure that the energy is exchanged among the DC capacitors. As already mentioned, due to the similarities of the second and third stages $T_{e3} = T_{e2}$, being T_{e3} the minimum time period the circuit should be kept in the third stage.

2.5.8 **Modelling of the fourth energizing stage**

Diagram 9 shows the equivalent circuit of the fourth energizing stage while Figure 10 (a) and Figure 10 (b) shows the waveforms of the DC voltages of phases "a", "b" and "c", and the MMC-STATCOM arm currents, where $V_{dc,a} = (V_{dc,a,upp} + V_{dc,a,\ell wr})$, $V_{dc,b} = (V_{dc,b,upp} + V_{dc,b,\ell wr})$ and $V_{dc,c} = (V_{dc,c,upp} + V_{dc,c,\ell wr})$, respectively.

Diagram 9 – Equivalent circuit for the fourth energizing stage.



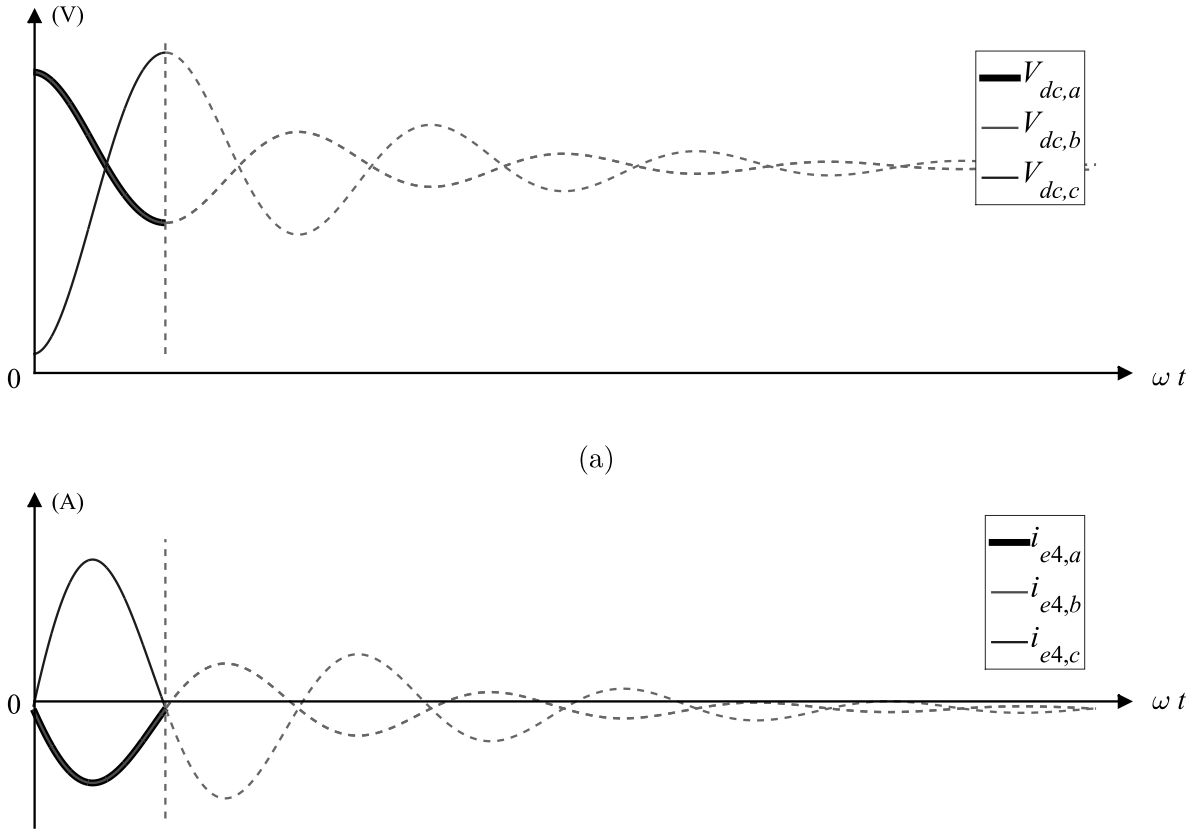
Source: Reproduced from (DUARTE; ALMEIDA; BARBOSA, 2019).

Again, due to the diodes of the IGBTs, the arm current of phase "c" does not become negative. Thus, the DC capacitors of phases "a" and "b" are discharged to energize the DC capacitors of phase "c", as shown in Figure 10.

The complex impedance, in the s-domain, of phases "a" and "b" of the equivalent circuit of Diagram 9 is given by:

$$Z_{e4,a}(s) = Z_{e4,b}(s) = 2n\left(R_C + \frac{1}{sC}\right) + sL_{eq,e4} + R_{eq,e4a}, \tag{2.20}$$

Figure 10 – Waveforms of the fourth energizing stage.



Caption: (a) DC voltages and (b) currents through the circuit.

Source: Elaborated by the author (2021).

where $L_{eq,e4} = 2L_f$ is the equivalent inductance and $R_{eq,e4a} = R_{eq,e4b} = (2nR_{igbt} + 2R_f)$ are the equivalent resistance of phases "a" and "b", respectively.

On the other hand, the complex impedance of phase "c", is given by:

$$Z_{e4,c}(s) = 2n\left(R_C + \frac{1}{sC}\right) + sL_{eq,e4} + R_{eq,e4c}, \tag{2.21}$$

where $R_{eq,e4c} = (2nR_D + 2R_f)$ is the equivalent resistance of phase "c".

Adding the parallel of the impedances of phases "a" and "b" to the impedance of phase "c" and making the final result equal to zero, yields:

$$\begin{aligned} s^2\left(3CL_fR_C\right) + s\left\{3L_f + 3CR_fR_C + nC\left[R_C\left(2R_D + R_{igbt}\right)\right]\right\} \\ +n\left(2R_D + R_{igbt}\right) + 3R_f = 0. \end{aligned} \tag{2.22}$$

Solving (2.22) for the frequency $s = (\sigma_{e4} + j\omega_{e4})$, the period of time of the fourth

energizing stage, is given by:

$$T_{e4} = \frac{1}{2}\left(\frac{2\pi}{\omega_{e4}}\right). \tag{2.23}$$

The value of T_{e4} is the minimum time period the circuit should be kept in the fourth energizing stage in order to ensure that the energy can be exchanged between the DC capacitors of the MMC-STATCOM.

2.5.9 The energizing controller of the MMC-STATCOM

It can be noted in Figure 5 that the longest time period of the first energizing stage occurs for the higher value of the DC voltage, that is, when the SM DC capacitors of the MMC-STATCOM are almost fully charged. On the other hand, the time period of the 2^{nd}, 3^{rd} and 4^{th} energizing stages are calculated by (2.19) and (2.23). Table 2 shows the time periods of each energizing stage of the MMC-STATCOM of Diagram 3 whose parameters are given by Table 9 in the Appendix A.

Table 2 – Time periods of the energizing stages

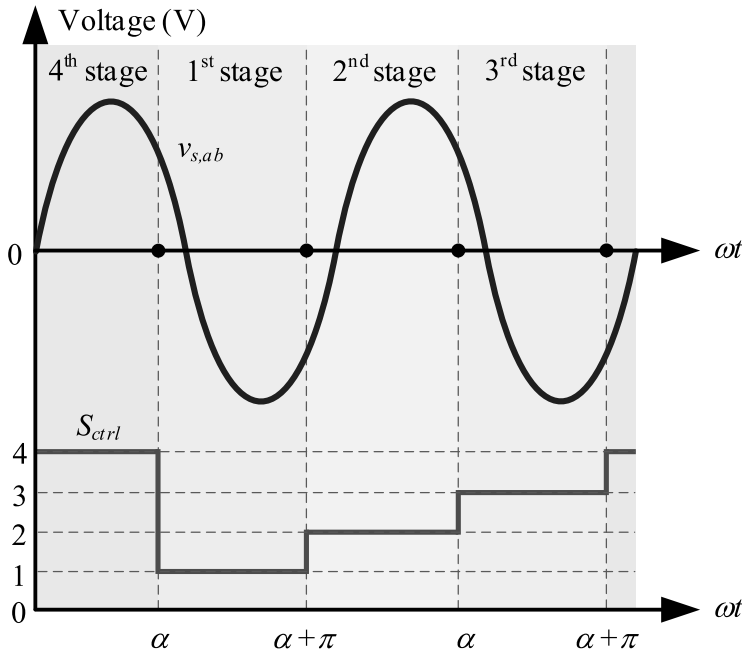
Parameter	**Value (ms)**
T_{e1}	3.55
T_{e2}	7.07
T_{e3}	7.07
T_{e4}	5.00

Source: Elaborated by the author (2021).

The sum of all time periods of the energizing stages given in Table 2 is 22.69 ms. Thus, the energizing stages of the MMC-STATCOM will be performed in two time periods of the grid voltage (40 ms = 2×(20 ms)), as shown in Figure 11, where the control signal S_{ctrl} is synchronized with the angle α and used to enable the energizing stages.

Diagram 10 shows the block diagram of the MMC-STATCOM's energizing controller. The angle ρ provided by a Phase-Locked Loop (PLL) is used by the block K_{ctrl} to generate the signal S_{ctrl}. This PLL is the same used during the operation of the MMC-STATCOM. More details on the PLL can be found in (RODRIGUEZ *et al.*, 2006). The angle ρ was 30° shifted to be synchronized with the line-to-line grid voltage. These signals are sent to the controllers of the four energizing stages (K_{e1}–K_{e4}). The DC voltage of a SM of the phase "a" lower arm is measured and multiplied by the number of SMs per converter arm n. After passing through a limiter, this signal is sent to the block PWL (2.14) whose output is the angle α. The angles α and ρ are then compared by the controllers K_{e1}–K_{e4} in order to generate the firing signals of the IGBTs and thyristors. For the MMC-STATCOM modelled in this chapter, the lower and upper limits of the voltage and angle limiters of Diagram 10 are (0 V and 34 kV) and (60° and 180°), respectively,

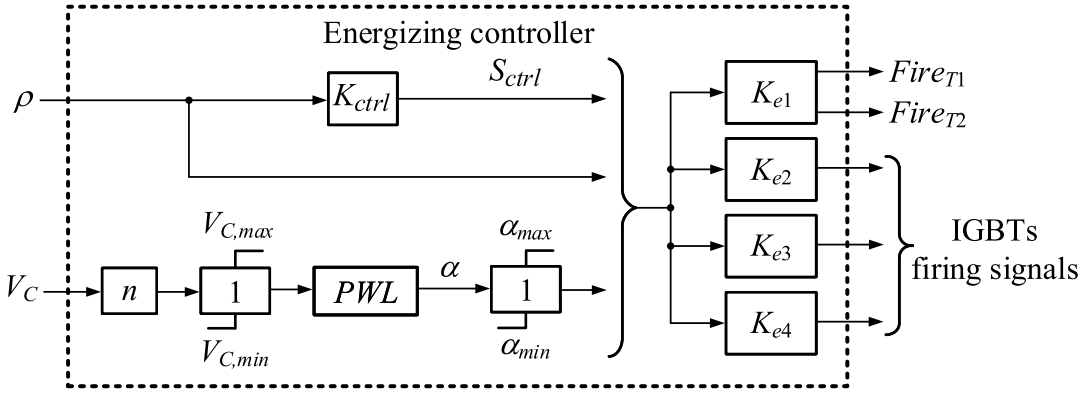
Figure 11 – The four energizing stages and its relations with the grid voltage.



Source: Elaborated by the author (2021).

being 34 kV ($= \sqrt{2}\times 24$ kV) the peak value of the network line-to-line voltage and, 60° and 180° the y-axis minimum and maximum angles of Figure 8, respectively.

Diagram 10 – Block diagram of the MMC-STATCOM energizing controller.

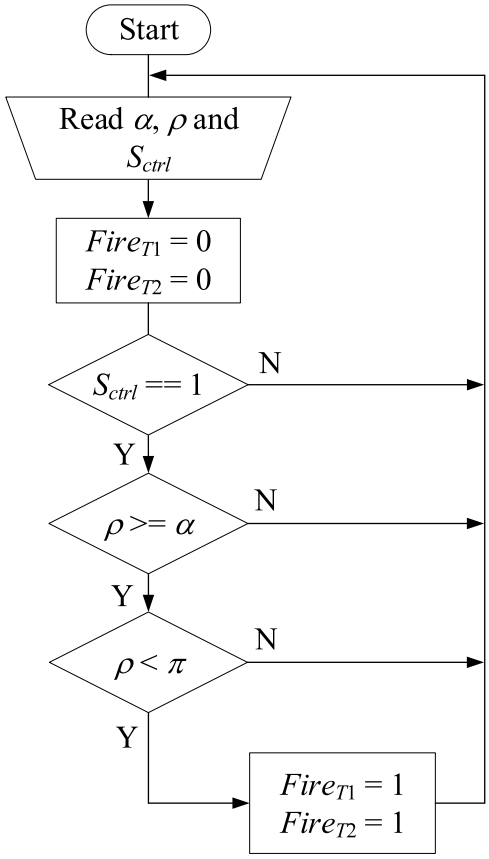


Source: Reproduced from (DUARTE; ALMEIDA; BARBOSA, 2019).

When the signal S_{ctrl} is equal to 1, the controller K_{e1} is enabled and the firing pulses of the thyristors $Fire_{T1}$ and $Fire_{T2}$ are used to control the current at the MMC-STATCOM terminals during the first stage. Flowchart 2 presents the logic of the controller K_{e1}. The logical levels 0 (zero) and 1 (one) of the signals $Fire_{T1}$ and $Fire_{T2}$ are used to represent the on and off states of the switches, respectively. If $S_{ctrl} = 2$ the controller K_{e2} turns on the switches ($S_{b1,1}$–$S_{b1,n}$) and ($S_{a2,n+1}$–$S_{a2,2n}$) during the second energizing stage. Flowchart 3 shows the logic of the controller K_{e2}. On the other hand, if $S_{ctrl} = 3$ the controller K_{e3}

turns on the switches ($S_{a1,n+1}$–$S_{a1,2n}$) and ($S_{b2,1}$–$S_{b2,n}$) during the third energizing stage. Flowchart 4 presents the logic of the controller K_{e3}. Finally, when S_{ctrl} is equal to 4, the controller K_{e4} turns on the switches ($S_{a1,1}$–$S_{a1,2n}$) and ($S_{b1,1}$–$S_{b1,2n}$) during the fourth energizing stage. The logic of the controller K_{e4} is presented in Flowchart 5.

Flowchart 2 – Flow chart of the controller K_{e1}.



Source: Elaborated by the author (2021).

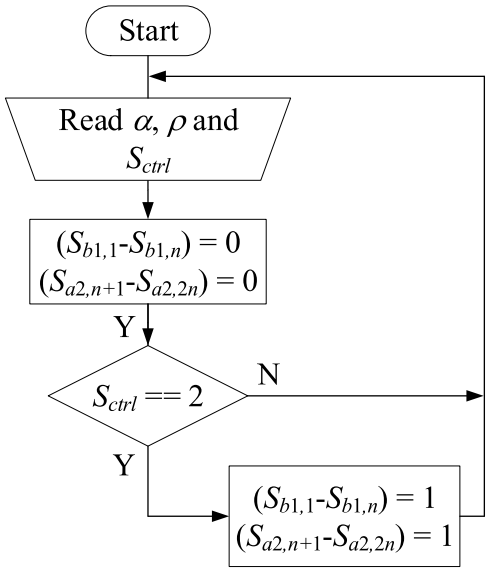
2.6 DIGITAL SIMULATION OF THE PROPOSED ENERGIZING STRATEGY

The circuit of Diagram 3 was modelled in an electromagnetic transient program to demonstrate and validate the energizing procedure proposed for the MMC-STATCOM. The grid and converter parameters are the same of those presented by Table 8 and Table 9, respectively, in the Appendix A.

2.6.1 **Pre-charge of the submodule DC capacitors using a PWL approximation with high number of breakpoints**

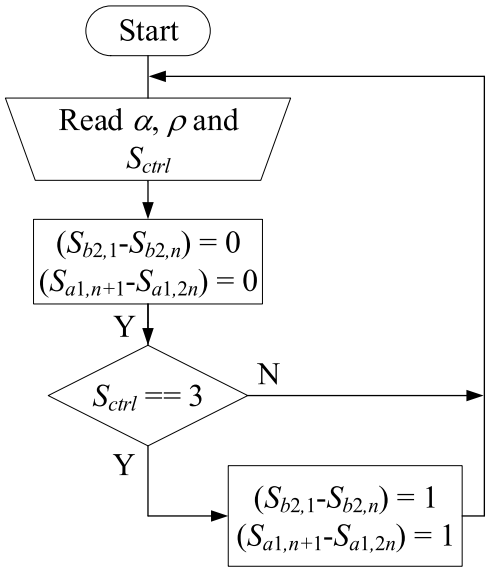
In the digital simulations presented in this subsection the thyristors of the energizing circuit are fired according to the PWL approximation of Figure 7, where the maximum

Flowchart 3 – Flow chart of the controller K_{e2}.



Source: Elaborated by the author (2021).

Flowchart 4 – Flow chart of the controller K_{e3}.

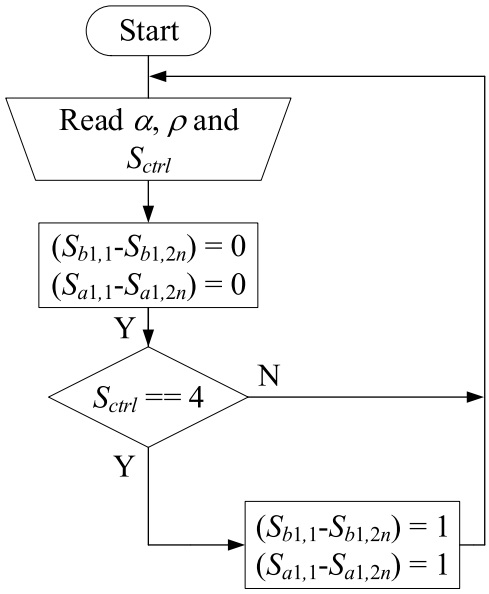


Source: Elaborated by the author (2021).

value of the energizing current is constant and equal to $I_{max} = 60$ A during all the energization procedure.

Figures 12 (a) and (b) show the waveforms of the thyristors firing angle and the current drained from the mains, respectively. As shown in Figure 12 (b), the peak value of the energizing current is constant during all the energizing procedure. This behaviour can be explained by the high number of breakpoints used in the PWL approximation, as

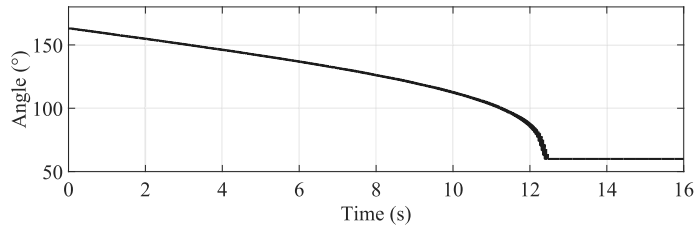
Flowchart 5 – Flow chart of the controller K_{e4}.



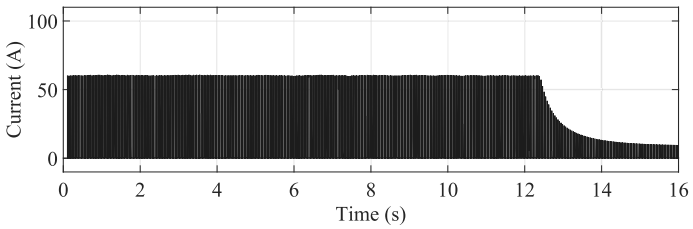
Source: Elaborated by the author (2021).

shown in Figure 7.

Figure 12 – Waveforms of the energizing circuit using the PWL approximation with high number of breakpoints (Figure 7).



(a)



(b)

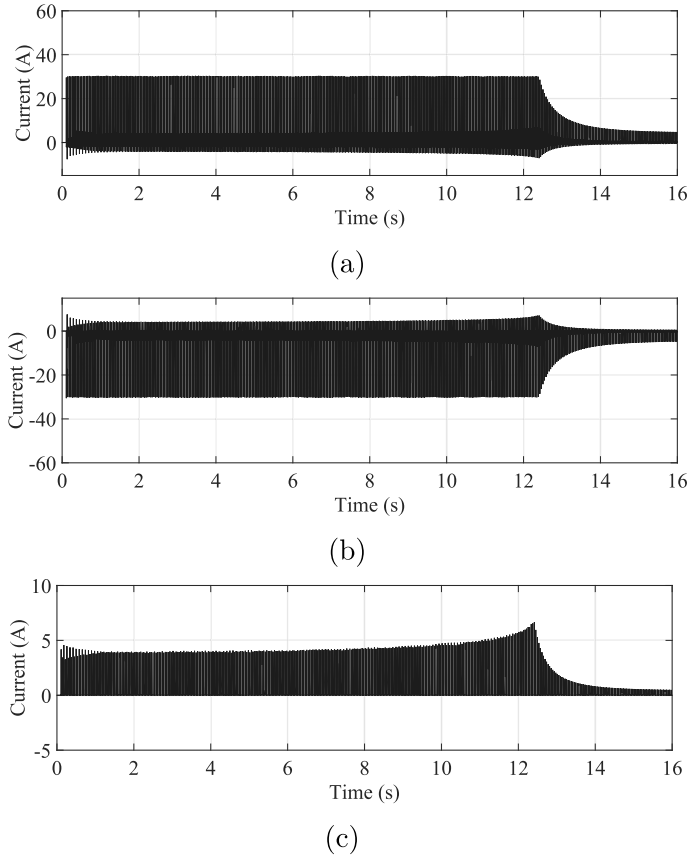
Caption: (a) firing angle of the thyristors and (b) phase "a" current drained from the electric network.

Source: Elaborated by the author (2021).

Figures 13 (a), (b) and (c) show the waveforms of the currents flowing through the lower arms of phases "a", "b" and "c" of the MMC-STATCOM, respectively. In order not

to compromise the visualization of the waveforms, the currents of the upper arms were omitted. As the current drained from the mains of Figure 12 (b), the peak value of the lower arm currents of the MMC-STATCOM, before the end of the energizing process, are constant.

Figure 13 – Waveforms of the lower arm currents of the MMC-STATCOM for the energizing process using the PWL approximation with high number of breakpoints (Figure 7).



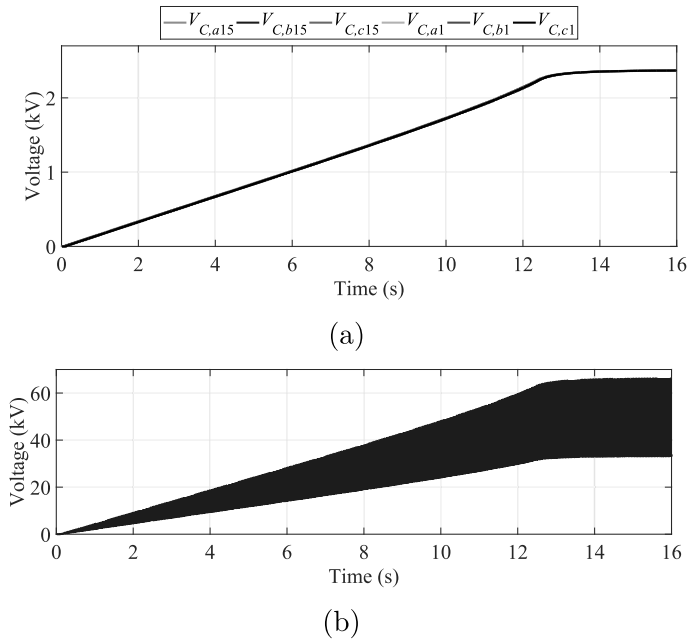
Caption: (a) phase "a", (b) phase "b" (c) phase "c".

Source: Elaborated by the author (2021).

Figures 14 (a) and (b) show the waveforms of the submodule DC capacitor voltages and the DC terminal voltage of the MMC-STATCOM, respectively. As the SM voltages of the same arm are equal, in Figure 14 (a) it is shown only the voltages of one SM of each upper and lower arm. It can be noted that the curves of the DC voltages of all SMs are superimposed. At the end of the energizing process, the capacitor voltages of the SMs will be approximately 2.4 kV($= \sqrt{2} \times 24$ kV$/14$), where 24 kV is the RMS value of the line-to-line network voltage and 14 is the number of SMs per arm of the MMC-STATCOM. The growth rate of the SM voltages depends on the peak value of the energizing current. The higher the energizing current value the higher the growth rate of the SM voltages and consequently the energizing process is faster.

Figure 15 shows a detail of the waveforms shown in Figure 12. The angle α

Figure 14 – Waveforms of the MMC-STATCOM DC voltages for the energizing process using the PWL approximation with high number of breakpoints (Figure 7).



Caption: (a) DC capacitor voltages of the lower and upper arms and (b) DC terminal voltage.

Source: Elaborated by the author (2021).

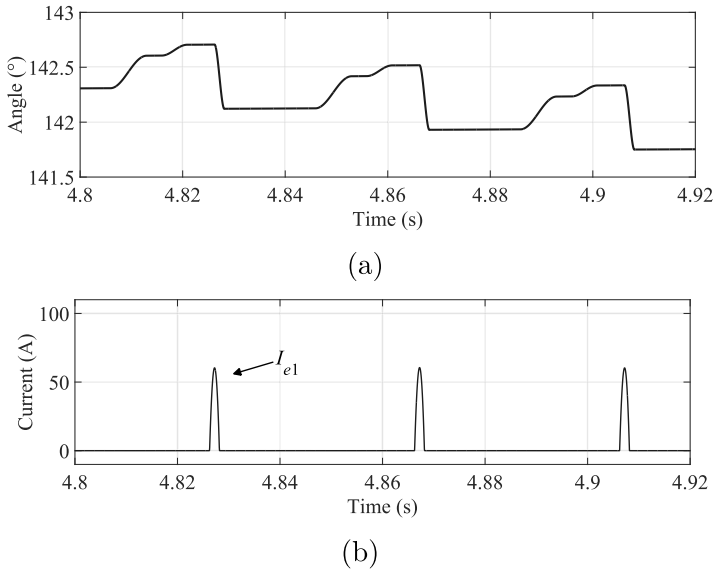
is computed by the energizing controller of Diagram 10 according to the methodology explained in the previous sections. The current pulse (i_{e1}), similar to that drawn in Figure 3 (Subection 2.4.1), flows through the converter's AC terminals after the thyristors are fired. This current charges the DC capacitors of the lower and upper arms of phases "a" and "b", respectively.

Figure 16 shows a detail of the waveforms shown in Figure 13. It can be noted that, during the first energizing stage, the peak value of the MMC-STATCOM arm currents are half of the current drained from the mains. After the first stage, the energy of the charged capacitors is exchanged between the other SM capacitors. The currents i_{e2}, i_{e3} and i_{e4} flow through the MMC-STATCOM DC capacitors during the 2$^{\text{nd}}$, 3$^{\text{rd}}$ and 4$^{\text{th}}$ energizing stages, respectively.

Figure 17 show a detail of the waveforms shown in Figure 14. Figure 17 (a) shows the energy exchange among the DC capacitors of the MMC-STATCOM during the 2$^{\text{nd}}$, 3$^{\text{rd}}$ and 4$^{\text{th}}$ energizing stages. It can be noted in Figure 17 (b) that the value of the MMC-STATCOM DC terminal voltage doubles every time the fourth energizing stage is enabled, since the upper and lower arms are connected in series.

Despite maintaining the peak value of the energizing current constant, the high number of breakpoint of the PWL approximation can increase the computational burden

Figure 15 – Waveform details of the energizing circuit using the PWL approximation with high number of breakpoints (Figure 7).



Caption: (a) firing angle of the thyristors and (b) phase "a" current drained from the electric network.

Source: Elaborated by the author (2021).

of the energizing algorithm. Therefore, in the next subsection the MMC-STATCOM will be energized according to a PWL approximation with low number of breakpoints.

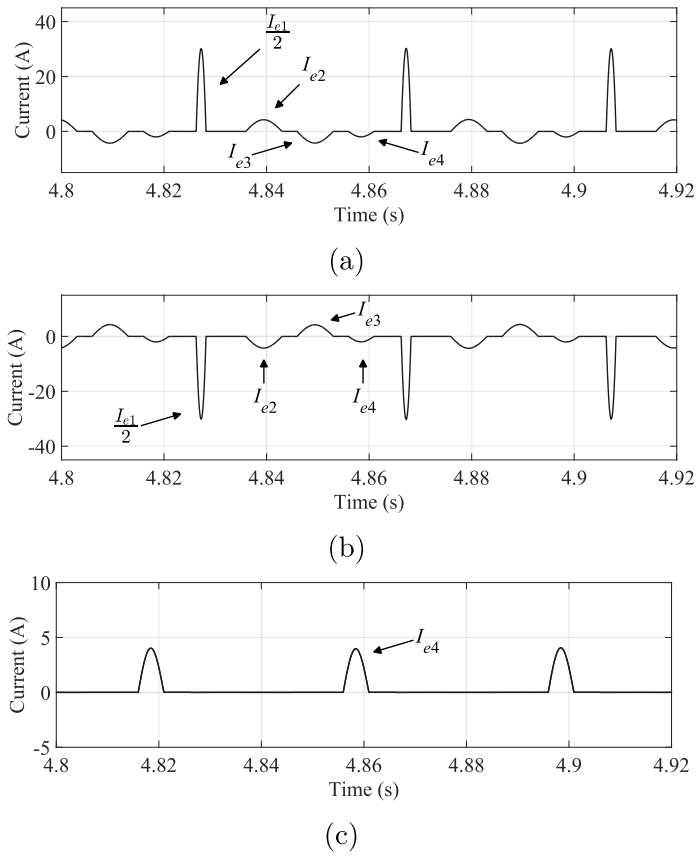
2.6.2 Pre-charge of the submodule DC capacitors using a PWL approximation with low number of breakpoints

In the digital simulations presented in this subsection the thyristors of the energizing circuit are fired according to the PWL approximation of Figure 8, where the maximum value of the energizing current is $I_{max} = 70$ A for $V_{dc} < 20$ kV and $I_{max} = 60$ A for $V_{dc} \geq 20$ kV.

Figures 18 (a) and (b) show the waveforms of the thyristor firing angle and the current drained from the mains, respectively. The energizing current slightly exceeds the $I_{max} = 70$ A for $t \leq 6$ s, however it does not surpass 80 A. This behaviour can be explained by the low number of points used in the PWL approximation, as shown in Figure 8. Otherwise, when V_{dc} is close to the breaking point value of the PWL approximation (see Figure 8), the energizing current maximum value is equal to I_{max}.

Figures 19 (a), (b) and (c) show the waveforms of the currents flowing through the lower arms of phases "a", "b" and "c" of the MMC-STATCOM, respectively. Figures 20 (a) and (b) show the waveforms of the submodule DC capacitor voltages and the DC terminal voltage of the MMC-STATCOM, respectively. Figure 21, Figure 22 and Figure 23 show waveform details of Figure 18, Figure 19 and Figure 20, respectively.

Figure 16 – Waveform details of the lower arm currents of the MMC-STATCOM for the energizing process using the PWL approximation with high number of breakpoints (Figure 7).



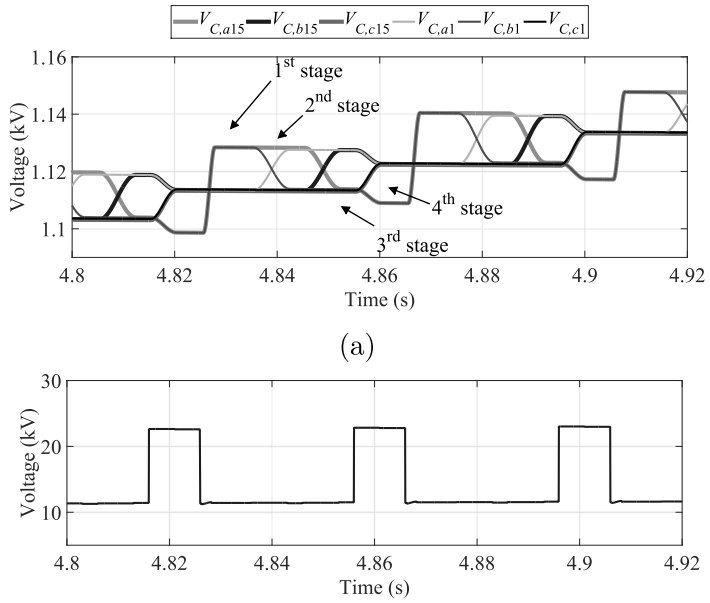
Caption: (a) phase "a", (b) phase "b" (c) phase "c".

Source: Elaborated by the author (2021).

It is important to mention that, during the 4$^{\text{th}}$ energizing stage, the DC capacitors of the upper and lower arm SMs of each phase are connected in series. Thus, at the end of the energizing process, considering that the capacitor voltages of the SMs will be approximately 2.4 kV ($= \sqrt{2} \times 24$ kV/14), the MMC-STATCOM DC terminal voltage will be approximately 67 kV ($= 28 \times 2.4$ kV) during the 4$^{\text{th}}$ energizing stage. Although this value is greater than the rated DC terminal voltage of the MMC-STATCOM (50 kV), the voltages over the capacitors, IGBTs and diodes will be smaller than the nominal value (3.57 kV = 50 kV/14).

The 34% of overvoltage on the DC terminals at the end of the energization process does not represent a critical problem for the operation of the MMC as STATCOM since the DC voltage of each SM is 33% smaller than its rated voltage. However, there are applications where the MMC is used as rectifier/inverter for an HVDC transmission system. In this example, the observed overvoltage can compromise the insulation of the cable or transmission line. Thus, in the following section, the energizing strategy proposed in

Figure 17 – Waveform details of the MMC-STATCOM DC voltages for the energizing process using the PWL approximation with high number of breakpoints (Figure 7).



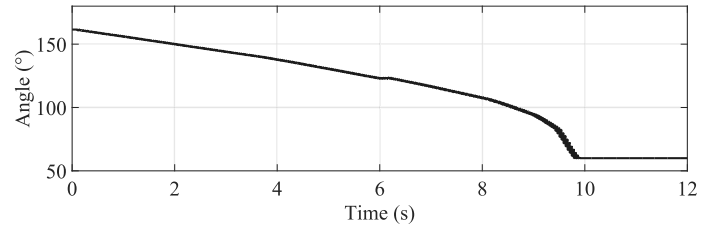
(a)

(b)

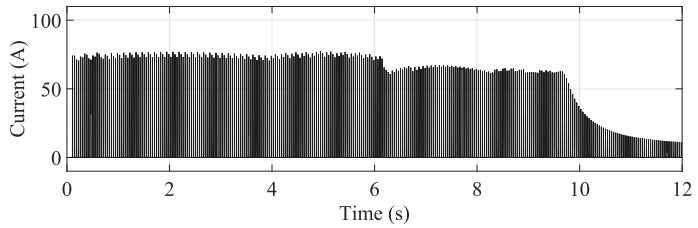
Caption: (a) DC capacitor voltages of the lower and upper arms and (b) DC terminal voltage.

Source: Elaborated by the author (2021).

Figure 18 – Waveforms of the energizing circuit using the PWL approximation with low number of breakpoints (Figure 8).



(a)

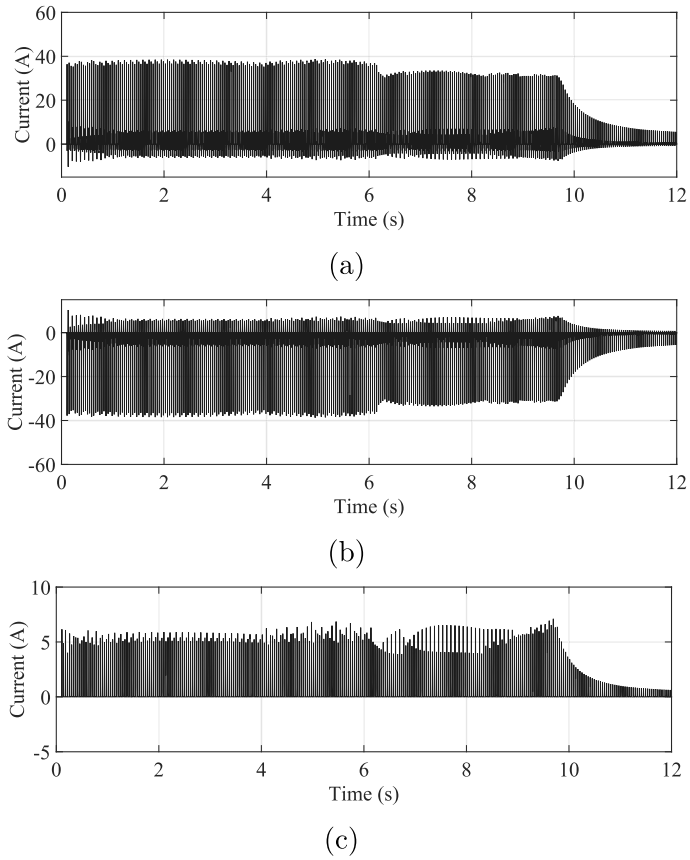


(b)

Caption: (a) firing angle of the thyristors and (b) phase "a" current drained from the electric network.

Source: Elaborated by the author (2021).

Figure 19 – Waveforms of the lower arm currents of the MMC-STATCOM for the energizing process using the PWL approximation with low number of breakpoints (Figure 8).



Caption: (a) phase "a", (b) phase "b" (c) phase "c".

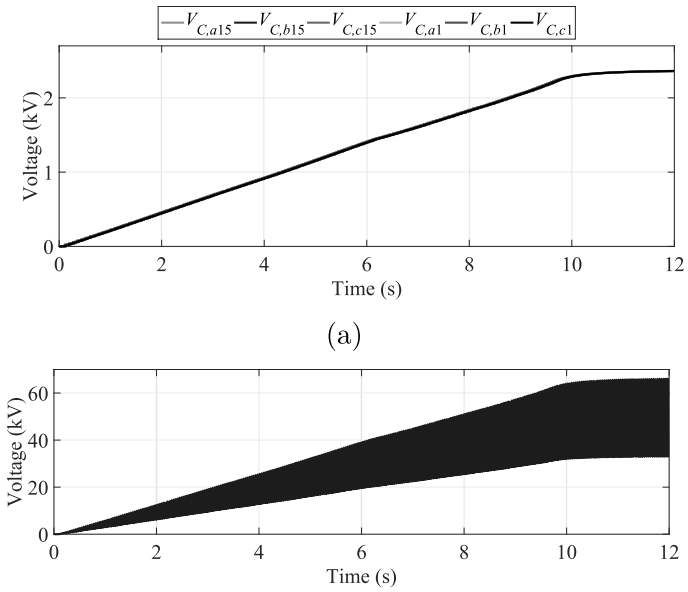
Source: Elaborated by the author (2021).

(DUARTE; ALMEIDA; BARBOSA, 2019) and presented in the previous sections will be improved in order to avoid overvoltage at the DC terminals of the MMC, as proposed in (DUARTE; ALMEIDA; BARBOSA, 2020).

2.7 MODIFICATION IN THE ENERGIZING STRATEGY TO AVOID OVERVOLTAGE AT THE DC TERMINALS OF THE MMC-STATCOM

The fourth stage of the energizing strategy, in which the lower and upper arms are connected in series, should be eliminated in order to avoid overvoltage at the DC terminals of the MMC-STATCOM, as shown in (DUARTE; ALMEIDA; BARBOSA, 2020). Thus, the charge of the SM capacitors of phase "c" can be made by connecting the upper SMs of phase "c" in parallel with those of phase "a", during the 2$^{\text{nd}}$ energizing stage. Likewise, the lower SMs of phase "c" can be connected in parallel with the lower SMs of phase "b" during the 3$^{\text{rd}}$ energizing stage. Besides the elimination of the 4$^{\text{th}}$ energizing stage, this scheme will allow to charge the capacitors of phase "c" without to exceed the rated DC

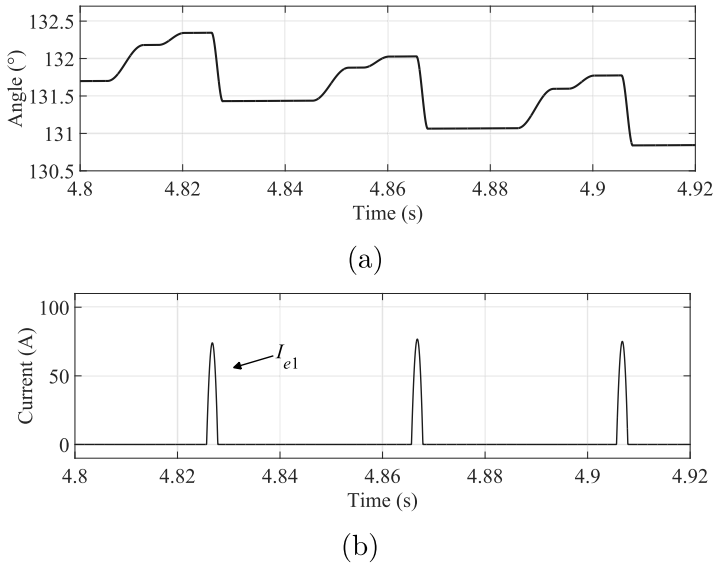
Figure 20 – Waveforms of the MMC-STATCOM DC voltages for the energizing process using the PWL approximation with low number of breakpoints (Figure 8).



Caption: (a) DC capacitor voltages of the lower and upper arms and (b) DC terminal voltage.

Source: Elaborated by the author (2021).

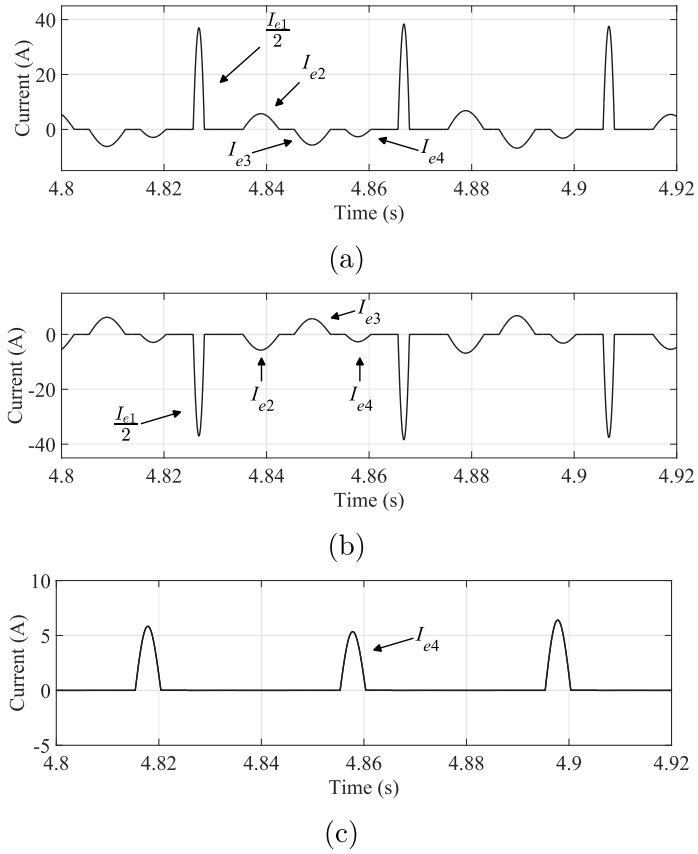
Figure 21 – Waveform details of the energizing circuit using the PWL approximation with low number of breakpoints (Figure 8).



Caption: (a) firing angle of the thyristors and (b) phase "a" current drained from the electric network.

Source: Elaborated by the author (2021).

Figure 22 – Waveform details of the lower arm currents of the MMC-STATCOM for the energizing process using the PWL approximation with low number of breakpoints (Figure 8).



Caption: (a) phase "a", (b) phase "b" (c) phase "c".

Source: Elaborated by the author (2021).

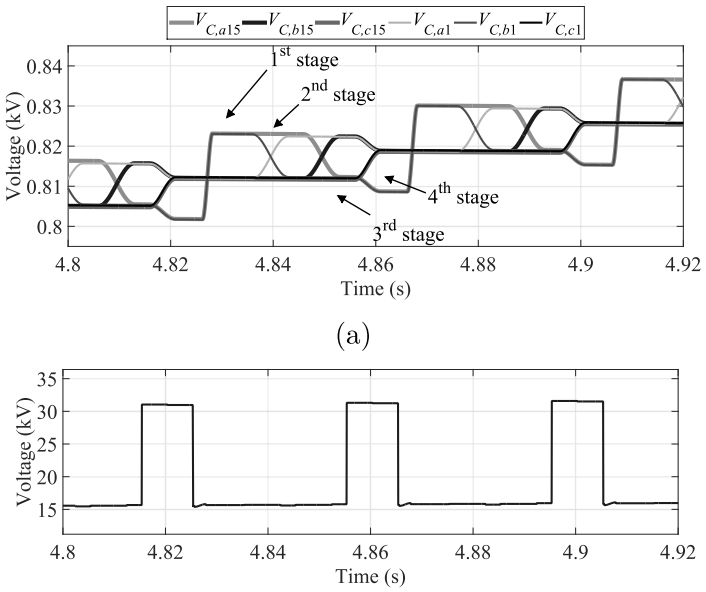
terminal voltage.

In the digital simulations presented in this section the thyristors of the energizing circuit are also fired according to the PWL approximation of Figure 8.

Figures 24 (a) and (b) show the waveforms of the thyristor firing angle and the current drained from the mains, respectively. Figures 25 (a), (b) and (c) show the currents flowing through the lower arms of phases "a", "b" and "c" of the MMC-STATCOM, respectively. Figures 26 (a) and (b) show the waveforms of the submodule DC capacitor voltages and the DC terminal voltage of the MMC-STATCOM, respectively.

Figure 27 and Figure 28 show a detail of the waveforms shown in Figure 24 and Figure 25, respectively. The currents i_{e2} and i_{e3} flow through the MMC-STATCOM DC capacitors during the 2$^{\text{nd}}$ and 3$^{\text{rd}}$ energizing stages, respectively. Their waveforms are shown in Figures 28 (a) and (b). It can be noted in Figure 28 (c) that the current of the 2$^{\text{nd}}$ and 3$^{\text{rd}}$ energizing stages flow through the lower arm SMs of phase "c".

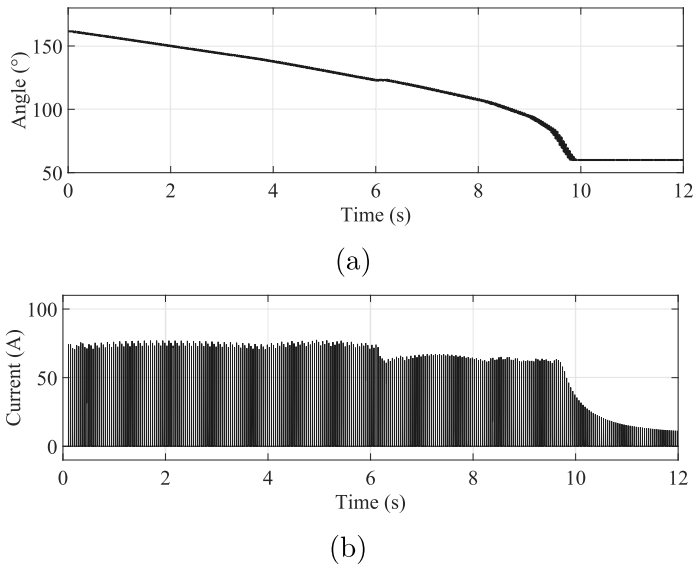
Figure 23 – Waveform details of the MMC-STATCOM DC voltages for the energizing process using the PWL approximation with low number of breakpoints (Figure 8).



Caption: (a) DC capacitor voltages of the lower and upper arms and (b) DC terminal voltage.

Source: Elaborated by the author (2021).

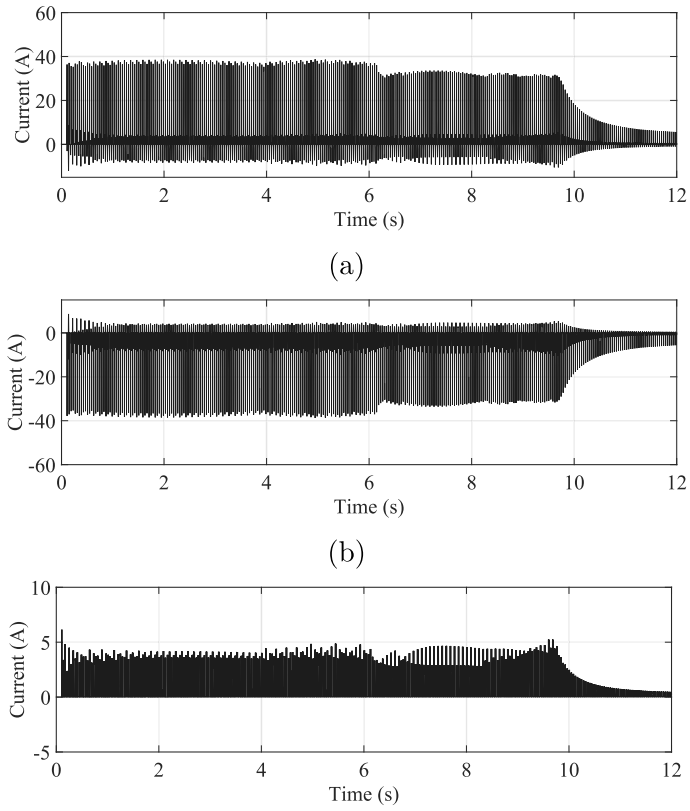
Figure 24 – Waveforms of the energizing circuit for the modified energizing strategy to avoid overvoltage at the DC terminals.



Caption: (a) firing angle of the thyristors and (b) phase "a" current drained from the electric network.

Source: Elaborated by the author (2021).

Figure 25 – Waveforms of the lower arm currents of the MMC-STATCOM for the modified energizing strategy to avoid overvoltage at the DC terminals.



Caption: (a) phase "a", (b) phase "b" (c) phase "c".

Source: Elaborated by the author (2021).

Figure 29 show a detail of the waveforms shown in Figure 26. It is possible to note in Figure 29 (a) that there are no fourth energizing stage. Furthermore, Figure 29 (b) shows that the DC terminal voltage does not double its value, since the upper and lower arms are not connected in series at any time.

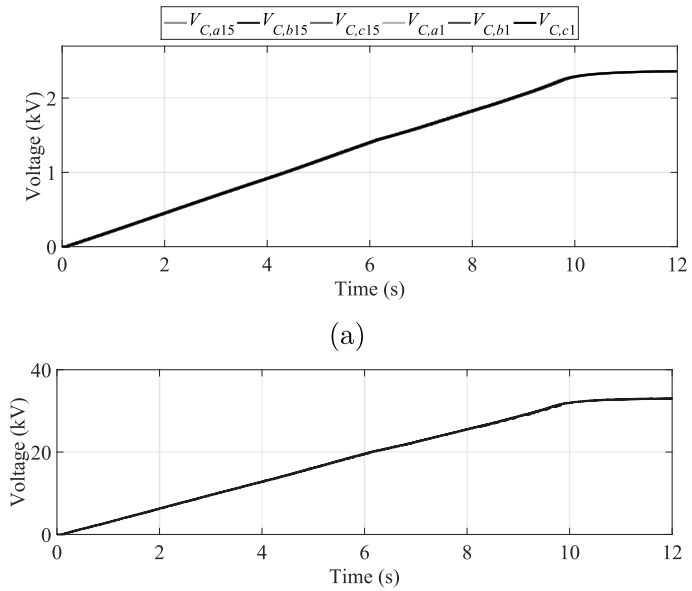
2.8 ADDITIONAL CONSIDERATIONS

This section presents additional considerations on the energizing strategy proposed for the MMC-STATCOM, such as impact on the PCC voltages, modification to energize a three-phase four-wire MMC-STATCOM, capacity of the thyristors of the energizing circuit, use of current limiting resistors and final charge of the SM DC capacitors.

2.8.1 **Impact of the energizing current on the PCC voltages**

Depending on the amplitude of the current drained from the grid during the energization of the MMC-STATCOM the voltages at the PCC can be very impacted.

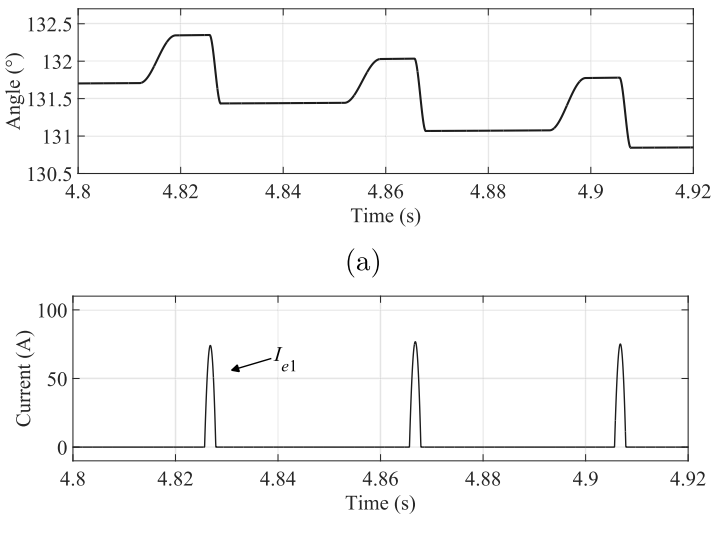
Figure 26 – Waveforms of the MMC-STATCOM DC voltages for the modified energizing strategy to avoid overvoltage at the DC terminals.



Caption: (a) DC capacitor voltages of the lower and upper arms and (b) DC terminal voltage.

Source: Elaborated by the author (2021).

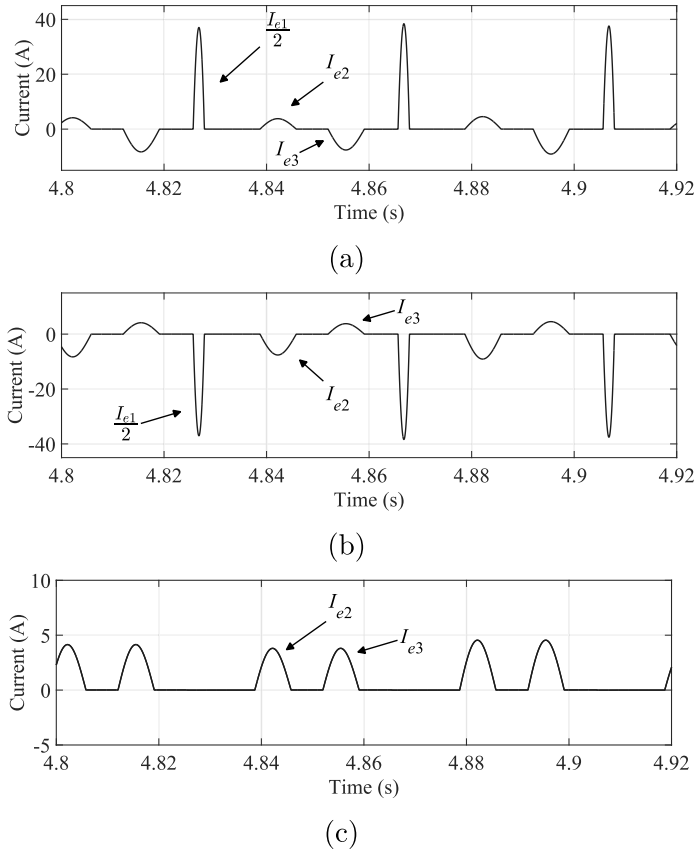
Figure 27 – Waveform details of the energizing circuit for the modified energizing strategy to avoid overvoltage at the DC terminals.



Caption: (a) firing angle of the thyristors and (b) phase "a" current drained from the electric network.

Source: Elaborated by the author (2021).

Figure 28 – Waveform details of the lower arm currents of the MMC-STATCOM for the modified energizing strategy to avoid overvoltage at the DC terminals.



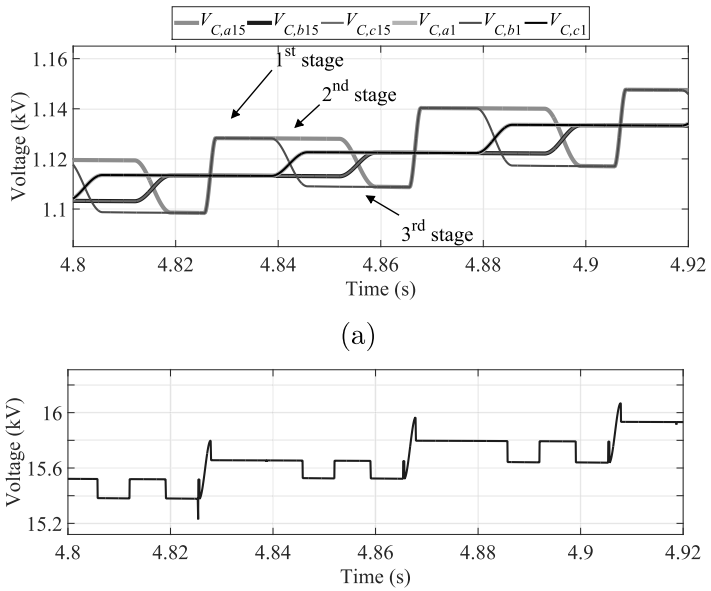
Caption: (a) phase "a", (b) phase "b" (c) phase "c".

Source: Elaborated by the author (2021).

Moreover, the smaller the network short-circuit power the lager the notch on the PCC voltages. Figure 30 (a) and (b) show a detail of the phase "a" terminal current of the MMC-STATCOM and the PCC voltages, respectively, when the submodule DC capacitors of the MMC-STATCOM are charged using the energizing strategy with three stages, as shown in Section 2.7. Again, the thyristors of the energizing circuit are fired according to the PWL approximation of Figure 8.

Its important to mention that the maximum value chosen for the energizing current ($I_{max} = 70$ A) of the MMC-STATCOM is lower than its nominal current (240 A). Moreover, the notch of 6.2% in the PCC voltages, measured in the waveform of Figure 30 (b), cannot be considered as a problem since according to the IEEE Standard 519 the notch depth limit for general systems is 20% (IEEE 519-2014, 2014).

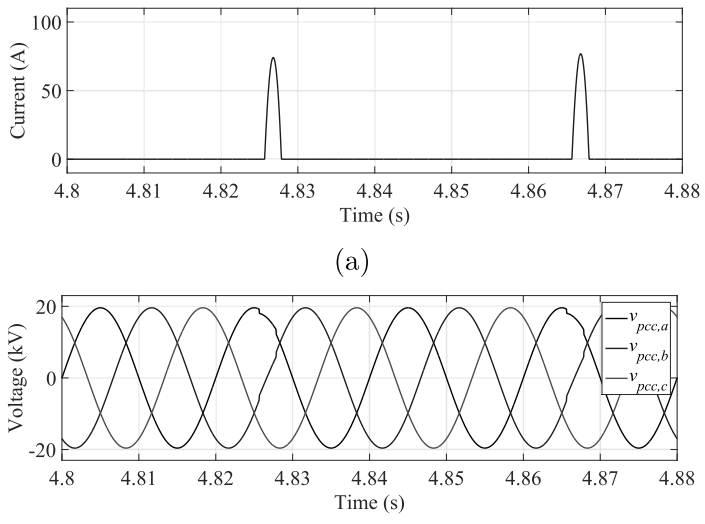
Figure 29 – Waveform details of the MMC-STATCOM DC voltages for the modified energizing strategy to avoid overvoltage at the DC terminals.



Caption: (a) DC capacitor voltages of the lower and upper arms and (b) DC terminal voltage.

Source: Elaborated by the author (2021).

Figure 30 – Waveform detail of the notch on the PCC voltages caused by the MMC-STATCOM energizing current.



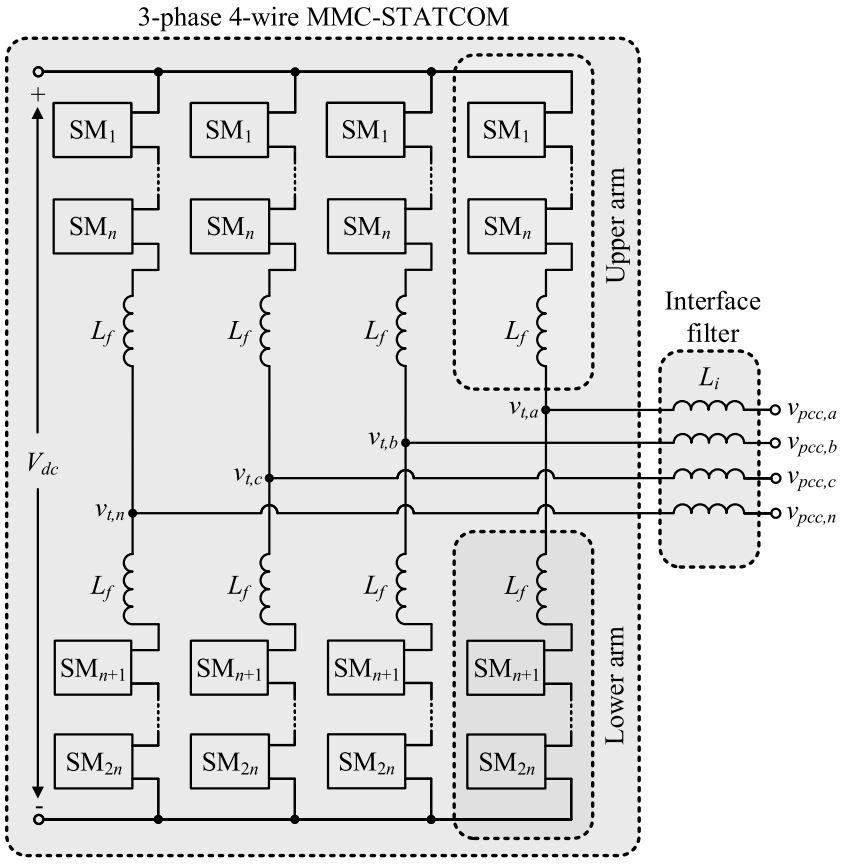
Caption: (a) MMC-STATCOM terminal current of phase "a" and (b) PCC voltages.

Source: Elaborated by the author (2021).

2.8.2 **Energization of three-phase four-wire MMC-STATCOM**

The energizing strategy presented in Section 2.4 can also be modified in order to energize a three-phase four-wire MMC-STATCOM, as proposed in (DUARTE; ALMEIDA; BARBOSA, 2020). Diagram 11 depicts the topology of the three-phase four-wire MMC-STATCOM. Each SM of the static compensator is also based on the half-bridge converter, as shown in Diagram 2. The SM capacitors of the fourth leg connected to the neutral can be charged in a similar way to the strategy presented in Section 2.7, where the fourth stage was eliminated. Then, considering the energization strategy with three stages, the charge of the SM capacitors of the neutral leg can be made by connecting the upper SMs of the neutral leg in parallel with those of phases "a" and "c", during the 2$^{\text{nd}}$ energizing stage. Likewise, the lower SMs of the neutral leg can be connected in parallel with the lower SMs of phases "b" and "c" during the 3$^{\text{rd}}$ energizing stage.

Diagram 11 – Topology of the three-phase four-wire MMC-STATCOM.



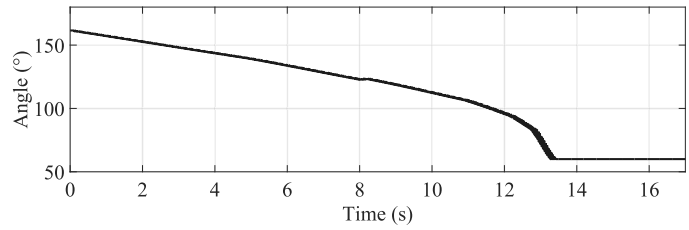
Source: Elaborated by the author (2021).

In the digital simulations presented in this subsection the thyristors of the energizing circuit are also fired according to the PWL approximation of Figure 8.

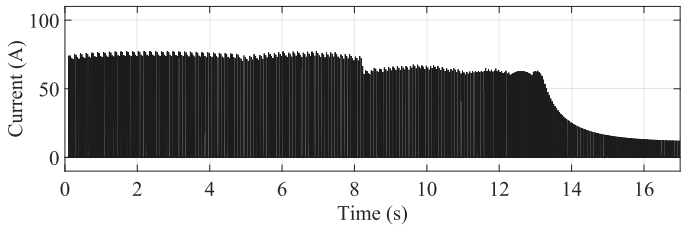
Figures 31 (a) and (b) show the waveforms of the firing angle of the thyristors and the current drained from the mains, respectively. Figures 32 (a) and (b) show the

currents flowing through the lower arms of phases "a" and "b" of the MMC-STATCOM, respectively. Figures 33 (a) and (b) show the waveforms of the currents flowing through the lower arms of phase "c" and neutral of the MMC-STATCOM, respectively. It can be noted that the currents through the phase "c" and neutral lower arms are identical, since in this modified energizing strategy the upper and lower arms of phase "c" and neutral are connected in parallel during the 2$^{\text{nd}}$ and 3$^{\text{rd}}$ stages, respectively. Figures 34 (a) and (b) show the waveforms of the submodule DC capacitor voltages and the DC terminal voltage of the MMC-STATCOM, respectively.

Figure 31 – Waveforms of the energizing circuit for the modified strategy to energize a three-phase four-wire MMC.



(a)



(b)

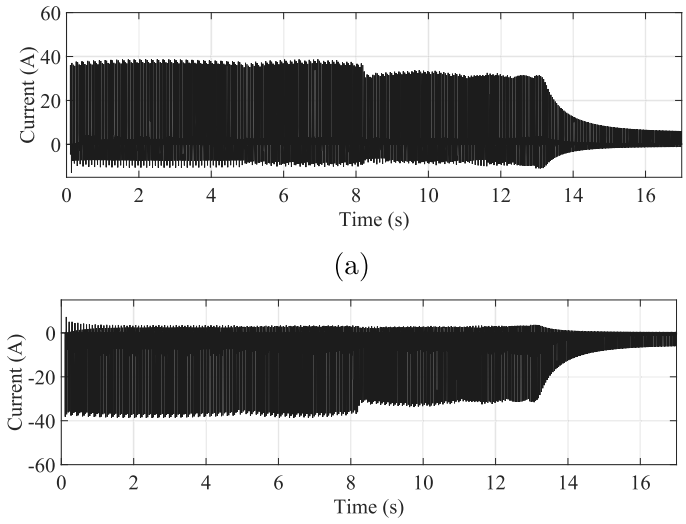
Caption: (a) firing angle of the thyristors and (b) phase "a" current drained from the electric network.

Source: Elaborated by the author (2021).

Figure 35, Figure 36 and Figure 37 show a detail of the waveforms displayed in Figure 31, Figure 32 and Figure 33, respectively. The currents i_{e2} and i_{e3} flow through the MMC-STATCOM DC capacitors during the 2$^{\text{nd}}$ and 3$^{\text{rd}}$ energizing stages, respectively. Their waveforms are shown in Figure 36 and Figure 37. It is possible to note that the currents of the 2$^{\text{nd}}$ and 3$^{\text{rd}}$ energizing stages flow through both lower arm SMs of phase "c" and neutral.

Figure 38 show a detail of the waveforms displayed in Figure 34. It can be noted in Figure 38 (a) that the SM capacitors of the neutral leg are charged together with the SM capacitors of phase "c".

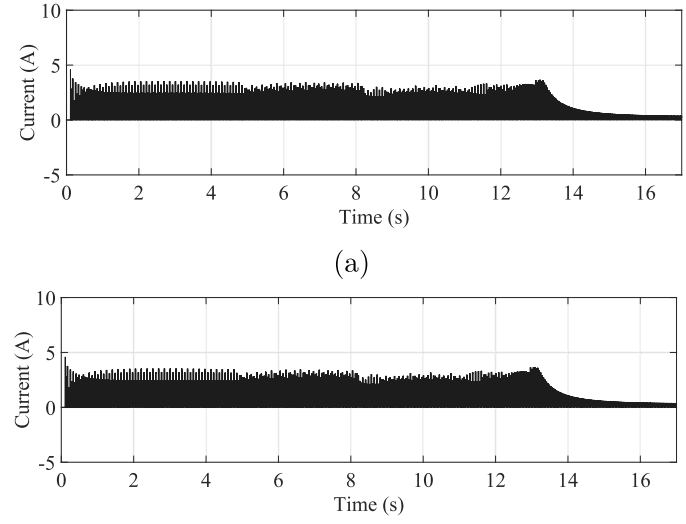
Figure 32 – Waveforms of the phases "a" and "b" lower arm currents of the STATCOM for the modified strategy to energize a three-phase four-wire MMC.



Caption: (a) phase "a" and (b) phase "b".

Source: Elaborated by the author (2021).

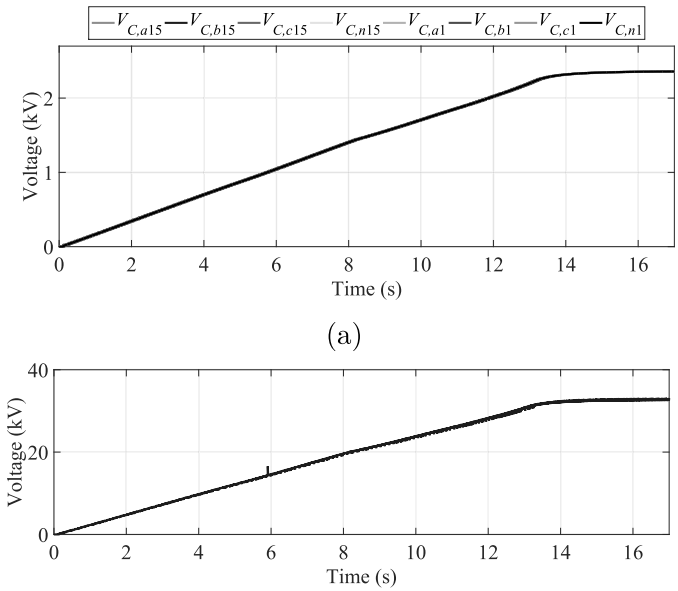
Figure 33 – Waveforms of the phase "c" and neutral lower arm currents of the STATCOM for the modified strategy to energize a three-phase four-wire MMC.



Caption: (a) phase "c" and (b) neutral.

Source: Elaborated by the author (2021).

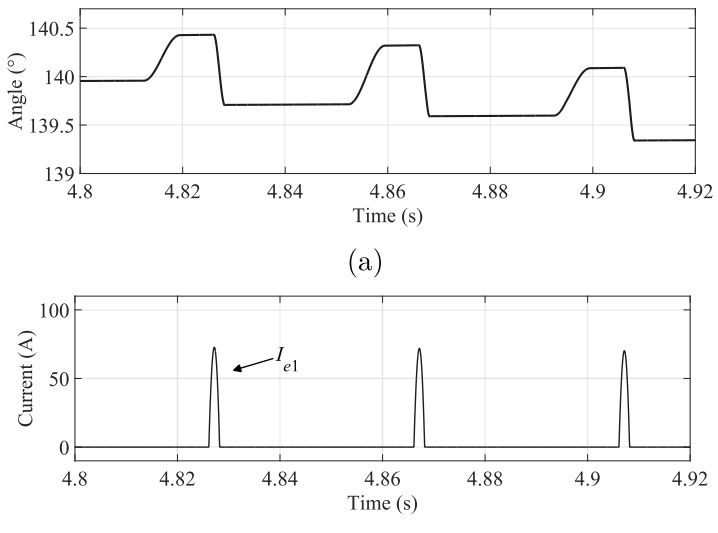
Figure 34 – Waveforms of the STATCOM DC voltages for the modified strategy to energize a three-phase four-wire MMC.



Caption: (a) DC capacitor voltages of the lower and upper arms and (b) DC terminal voltage.

Source: Elaborated by the author (2021).

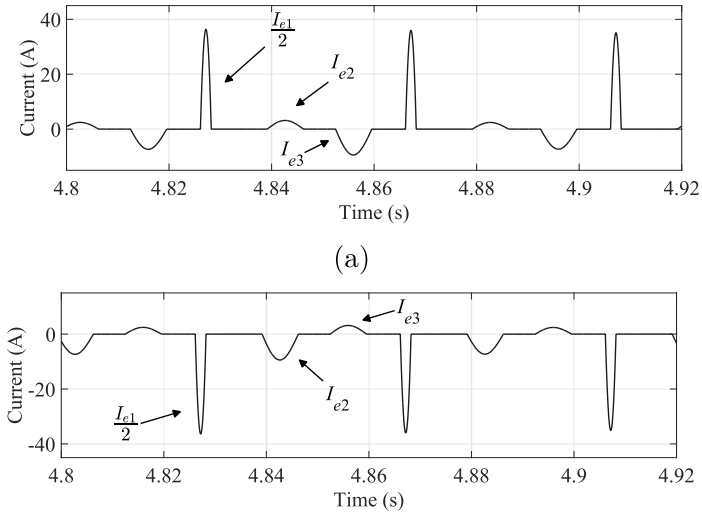
Figure 35 – Waveform details of the energizing circuit for the modified strategy to energize a three-phase four-wire MMC.



Caption: (a) firing angle of the thyristors and (b) phase "a" current drained from the electric network.

Source: Elaborated by the author (2021).

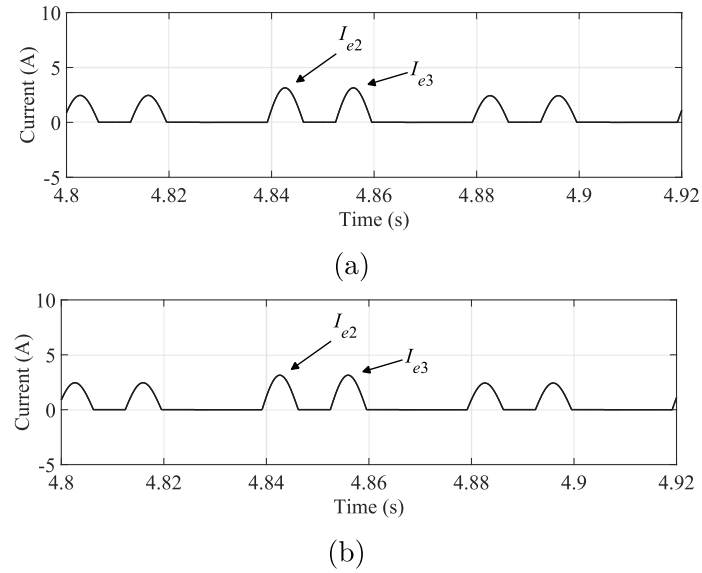
Figure 36 – Waveform details of the phases "a" and "b" lower arm currents of the STATCOM for the modified strategy to energize a three-phase four-wire MMC.



Caption: (a) phase "a" and (b) phase "b".

Source: Elaborated by the author (2021).

Figure 37 – Waveform details of the phase "c" and neutral lower arm currents of the STATCOM for the modified strategy to energize a three-phase four-wire MMC.



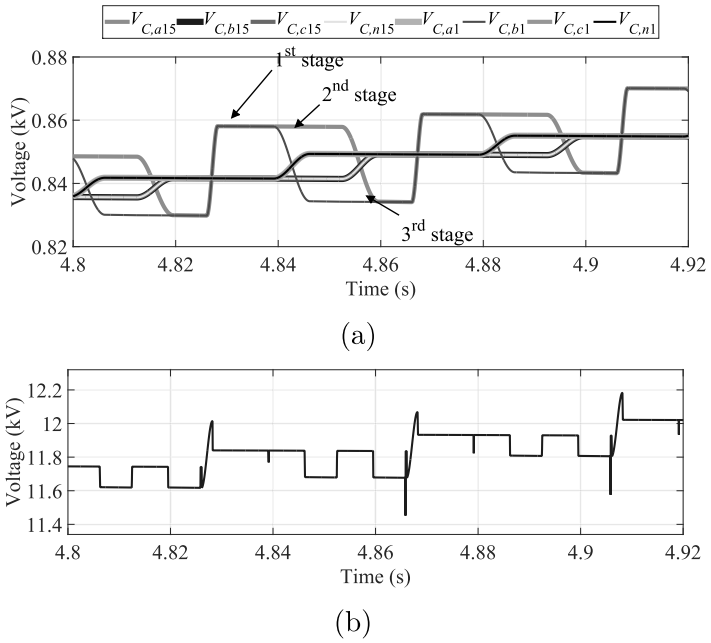
Caption: (a) phase "c" and (b) neutral.

Source: Elaborated by the author (2021).

2.8.3 **Considerations on the capacity of the thyristors used in the energization circuit**

As in the case of other power devices, the thyristors will only have a safe operation if they are not subjected to electrical and thermal stress. Many of the electrical quantities

Figure 38 – Waveform details of the STATCOM DC voltages for the modified strategy to energize a three-phase four-wire MMC.



Caption: (a) DC capacitor voltages of the lower and upper arms and (b) DC terminal voltage.

Source: Elaborated by the author (2021).

specified in the thyristors datasheets are given for the worst possible case, that is, when the semiconductor junction temperature is at the permissible maximum value (RASHID, 2017). These constrains are applied to the maximum repetitive peak forward and reverse blocking voltage as well as the RMS, average and peak on-state currents through the thyristors. Table 3 gives the values simulated for the thyristors used in the energizing circuit of Diagram 3. The maximum peak forward and reverse voltages can be derived from the equivalent circuits of Diagram 3, Diagram 4, Diagram 5 and Diagram 6. On the other hand, the RMS, average and peak values of the currents through the thyristors are obtained from the waveform shown in Figure 27 (a). Depending on the values of the grid voltage and energizing current an association of thyristors can be performed to compose the switches.

2.8.4 **Comparison between the proposed energizing strategy and the use of current limiting resistors**

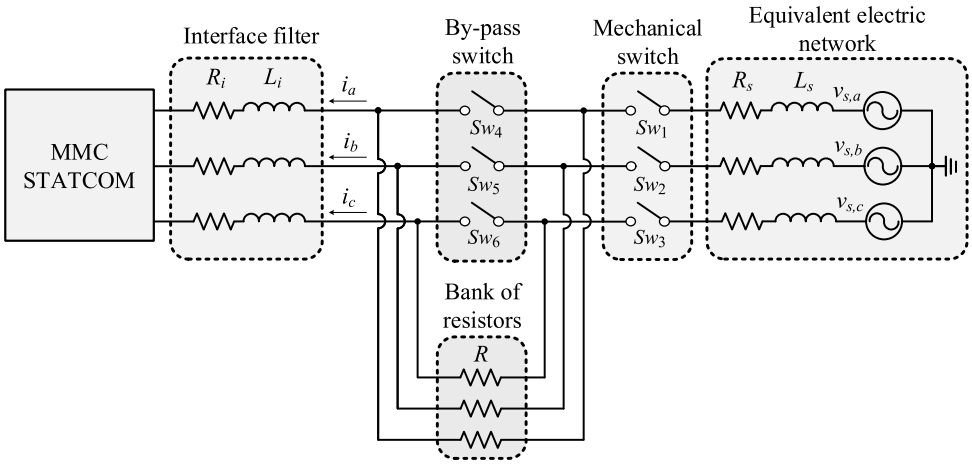
For comparison purposes, the three-phase three-wire MMC-STATCOM was connected to the mains through three pre-charge resistors. Diagram 12 depicts the new system configuration where three auxiliary switches bypass the resistors after the pre-energization of the SM DC capacitors.

Table 3 – Thyristors' requirements

Parameter	Value
Maximum repetitive peak forward voltage (V_{FB})	19.6 kV
Maximum repetitive peak reverse voltage (V_{RB})	19.6 kV
RMS on-state current (I_{FRMS})	12.5 A
Average on-state current (I_{FAV})	3.2 A
Peak on-state current (I_F)	70 A

Source: Reproduced from (DUARTE; ALMEIDA; BARBOSA, 2019).

Diagram 12 – MMC-STATCOM connected to the electric network through pre-charge resistors.

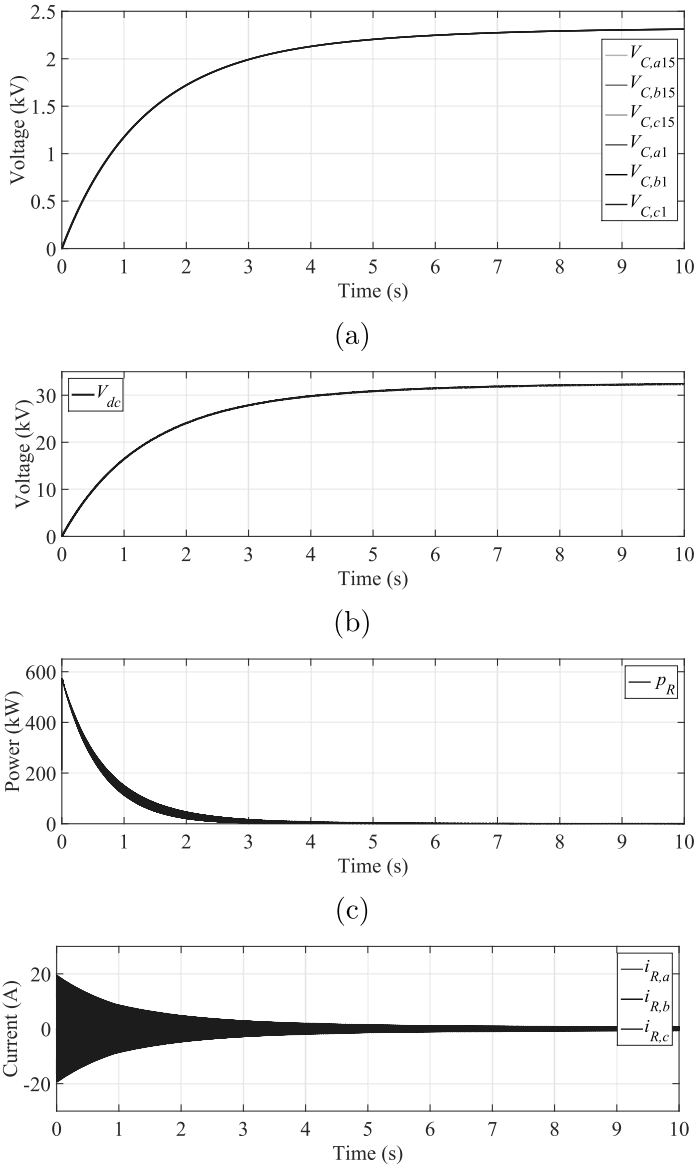


Source: Adapted from (DUARTE; ALMEIDA; BARBOSA, 2019).

The pre-charge resistors were designed with a resistance of 1 kΩ, so that the charging time of the DC capacitors is somewhat close to that one observed when the proposed energizing circuit is used to charge the DC capacitors of the MMC-STATCOM. Figures 39 (a), (b), (c) and (d) show the waveforms of the MMC-STATCOM upper and lower arm SM voltages, the MMC-STATCOM DC terminal voltage, the power dissipated by the resistors during the pre-charge of the MMC-STATCOM DC capacitors and the three-phase currents through the resistors. The total energy dissipated during the pre-charge can be numerically calculated by integrating the power curve of Figure 39 (c), resulting in approximately 576 kJ.

On the other hand, when the proposed circuit is used, no current flows through the thyristors when they are blocked. Then, bearing in mind the RMS and average values of the energizing current given in Table 3, assuming a forward voltage drop equal to 1.5 V and a dynamic resistance of 5 mΩ for T_1 and T_2 and considering also that each valve is formed by 3 thyristors connected in series, the power dissipated by the thyristors will be approximately 33.49 W ($= 2 \times 3 \times 1.5$ V $\times$ 3.2 A $+ 2 \times 3 \times 5$ mΩ $\times$ (12.5 A)^2).

Figure 39 – Waveforms of the MMC-STATCOM DC voltages and the power loss of the current limiting resistors.



Caption: (a) MMC-STATCOM upper and lower arm SM voltages, (b) MMC-STATCOM DC terminal voltage, (c) power loss of the current limiting resistors and (d) three-phase currents through the resistors.

Source: Elaborated by the author (2021).

Then, considering an energization time equal to 10 s as shown in Figure 25, the total energy dissipated by the thyristors will be approximately 334.9 J. That is, the energy dissipated by the proposed circuit is 0.058% (approximately 1700 times smaller) of the energy dissipated when resistors are used.

In addition to the comparison of dissipated power, the following topics can be cited

as advantage of the proposed energizing strategy compared to the use of current limiting resistors:

- The energizing current present a constant peak value during all the proposed energizing procedure;
- The energizing current can be reduced controlling the firing angle of the thyristors, while in the other strategy the current limiting resistors should be replaced;
- The additional by-pass mechanical switch is not necessary in the proposed strategy;
- Depending on the parameters of the circuit, resistors with high thermal capacity may be required when they are used to limit the energizing current.

2.8.5 **The final charge of the submodule DC capacitors**

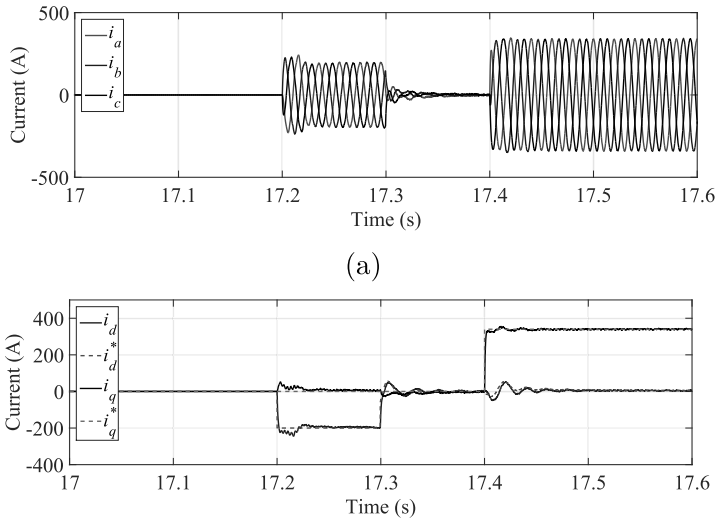
After the pre-charge of the three-phase three-wire MMC-STATCOM DC capacitors of Diagram 2 by using the proposed energizing circuit, as shown in Section 2.7, the converter DC terminal voltage is equal to the peak value of the mains line-to-line voltage. Then, the thyristors T_1 and T_2 are blocked, the mechanical contacts Sw_1, Sw_2 and Sw_3 are closed (refer Diagram 3) and the energizing circuit is disabled. From this point forward, two controllers designed in the synchronous reference frame regulate the currents synthesized by the MMC-STATCOM. These controllers are used here only to demonstrate the transition between the energizing process and the operation of the MMC as STATCOM. More details on the design of these controllers will be presented in Section 3.2.

Figures 40 (a) and (b) show the currents at the MMC-STATCOM output terminals, the reference signals (dashed-line) and the synthesized currents in dq reference frame, respectively. Figures 41 (a) and (b) show the DC capacitor voltages of the upper and lower arm SMs and the DC terminal voltage of the MMC-STATCOM, respectively. In $t = 17.2$ s the reference signal i_d^* is varied to -200 A to force the MMC-STATCOM to absorb active power from the grid in order to charge the SM capacitors. The initial value of the SM voltages are approximately 2.3 kV. This value was reached due to the pre-charge strategy presented in Section 2.4. It can be noted that the voltages of the DC capacitors increase linearly from $V_{dc} = 2.3$ kV to the SM capacitor rated voltage $V_{dc} = 3.57$ kV. In $t = 17.4$ s the reference signal i_q^* is step changed from 0 to +340 A to force the MMC-STATCOM to start compensating reactive power at its terminals.

2.9 CONCLUSIONS

This chapter presented an energizing strategy for a grid-connected three-phase modular multilevel converter operating as static synchronous compensator. The energizing circuitry is composed of a controller and two thyristors. Since the thyristors were connected

Figure 40 – Waveforms of the MMC-STATCOM currents during the final charge of the SM capacitors.



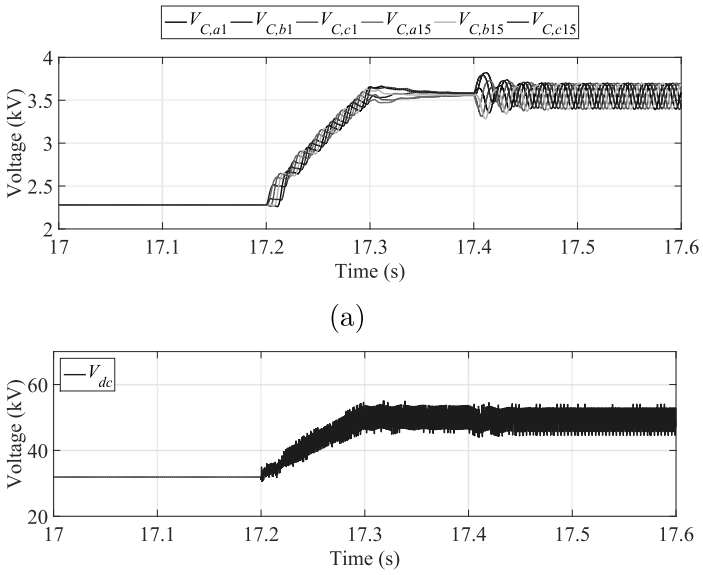
(a)

(b)

Caption: (a) three-phase terminal currents and (b) i_d and i_q and the respectively reference signals.

Source: Elaborated by the author (2021).

Figure 41 – Waveforms of the MMC-STATCOM DC voltages during the final charge of the SM capacitors.



(a)

(b)

Caption: (a) DC voltages of the lower and upper arm SM capacitors and (b) DC terminal voltage.

Source: Elaborated by the author (2021).

in parallel to the contacts of the mechanical switch used to connect the MMC-STATCOM to the grid, no topological change was required to implement the energizing circuitry. During the first stage of the energizing processes the capacitors of the lower arm SMs of phase "a" and upper arm SMs of phase "b" were charged by the current drained from the grid. The equivalent circuit for the 1st energizing stage was modelled and used to derive mathematical relations to determine the peak value of the energizing current as a function of the thyristors firing angle. A routine based on the Newton-Raphson method was used to solve numerically the non-linear equation for different values of V_{dc}, returning the firing angles to keep the peak value of the energizing current constant and equal to a predefined value. A piecewise linear technique was used to approximate the obtained non-linear characteristic curve in order to reduce the computational burden of the energizing current control during the 1st stage. During the following energizing stages the other DC capacitors were charged by means of an energy exchange with the capacitors already charged during the 1st stage. Since the thyristors were kept blocked during these steps, the energy exchange between the SM capacitors was accomplished by activating some specific IGBTs at each energization stage to provide a path for the current flow. Again no topological change or additional components was required since only the activation sequence of the IGBTs of the MMC-STATCOM was changed. This characteristic constitutes another advantage of the proposed method. As disadvantage of the proposed strategy it can be cited the harmonics and the DC component of the energizing current drained from the network. However, as the maximum value of the energizing current can be controlled by the firing pulses of the thyristors, these problems could be minimized. Different from others energizing strategies proposed in the literature, no additional passive elements (resistances or inductances), transformers or DC sources were used in the proposed strategy. Moreover, as the mechanical switch used to connect the MMC-STATCOM to the grid was also used in the proposed energizing circuit, no additional mechanical switches were necessary. The methodology presented in this chapter can also be easily adjusted to energize MMC-STATCOMs with any number of SMs per arm, since the IGBTs of the SMs in the same arm should be switched with the same pattern. The results of digital simulations were used to validate the theoretical equations and to demonstrate the proposed energizing strategy. In the next chapters of this thesis the MMC-STATCOM will be considered fully energized.

3 NEGATIVE-SEQUENCE VOLTAGE COMPENSATION OF A DISTRIBUTION NETWORK THROUGH A THREE-PHASE THREE-WIRE MMC-STATCOM

Another objective of this thesis is to present positive-, negative- and zero-sequence network voltage compensation strategies in distribution networks by using the MMC-STATCOM.

This chapter presents the methodology published in Duarte *et al.* (2021) to control the MMC-STATCOM in order to regulate the positive-sequence and to compensate the negative-sequence voltages at the PCC of a distribution network. The mathematical models used to derive the positive- and negative-sequence current and voltage control loops for the MMC-STATCOM will be shown. In addition, results of digital simulations will be used to demonstrate the effectiveness of the compensation algorithm.

Although the introduction of this chapter deals with voltage imbalance in distribution networks, that is negative- and zero-sequence voltages, for the sake of organization of this thesis the zero-sequence voltage compensation will be presented only in Chapter 4.

3.1 INTRODUCTION

In the last two decades, the power quality of the distribution networks has become a very discussed topic in several forums and conferences around the world. This subject has motivated the publication of several books and scientific papers, describing many of the observed power quality problems and possible solutions to compensate them (BOLLEN, 2000; ARRILLAGA; WATSON, 2004; SINGH; CHANDRA; AL-HADDAD, 2015). Concerned about the severity and recurrence of power quality problems, technical organizations and regulatory agencies in different countries have established indexes to assess the quality of the energy supplied and consumed, in addition to rules for accessing resources in their electrical networks (IEEE 519-2014, 2014; IEC, 2008).

Modern distribution networks provide electricity for a variety of linear and non-linear loads which are connected to one, two and three phases of the network. These loads drain unbalanced and distorted currents from the feeders, unbalancing the supply voltage and compromising the power quality of the system (IEC, 2008; JOUANNE; BANERJEE, 2001; ARAUJO *et al.*, 2013). In addition to different types and values of load impedance connected to each system's phase, unbalanced voltages can also be caused by: (*i*) points of bad contacts; (*ii*) large single-phase distribution transformers; (*iii*) open phase on the primary side of a three-phase transformer; (*iv*) faults in the power transformers; (*v*) open phase of a capacitor bank; (*vi*) unequal impedance in the feeders; (*vii*) heavy reactive single-phase loads such as welders, among others (JOUANNE; BANERJEE, 2001; MEERSMAN *et al.*, 2009).

A recently published work investigated the strategies proposed in the past two

decades to mitigate imbalances in distribution networks (VIJAY; DOOLLA; CHANDORKAR, 2020). In addition to reporting a rising trend in research on this topic, the authors presented a summary of the recommendations made by the main organisations regarding imbalances, which are quantified using different methodologies (PILLAY; MANYAGE, 2001). In order to exemplify some differences between the guidelines, according to the American National Standard Institute (ANSI) (ANSI Standard, 2011), the voltage unbalance of a power system should not be greater than 3%, while the International Electrotechnical Commission (IEC) (IEC, 2008) recommends that the voltage imbalance in the electric networks does not exceed 2%. Others organizations propose several indexes. For instance, the National Electrical Manufacturers Association (NEMA) recommends that the voltage imbalance at the electrical motors' terminals should be less than 1% (NEMA Standards Publication MG 1-2016, 2016).

Unbalanced voltages can cause serious problems in various electrical devices, especially in electric motors. The presence of negative- and zero-sequence components on the supply voltages produces pulsating torques and speed variations on the motors shafts. In addition, excessive voltage unbalance causes over currents that increase the heat production due to joule and magnetic losses, shortening the motor's life and possibly causing its burning in extreme cases (FUCHS; MASOUM, 2015). Imbalances can also be responsible for disruption in industries and companies. As an example, considering a printing company where sheets and rolls of paper are driven by electric motors, the presence of pulsating torques can cause the de-synchronization of printing process leading to loss of the production.

These problems tend to become worse in the near future, when considering a scenario with high penetration of distributed generation resources, specially those based on alternative energy source such as the single-phase rooftop photovoltaic systems (ALMEIDA *et al.*, 2016; RUIZ-RODRIGUEZ; HERNÁNDEZ; JURADO, 2015; YAN *et al.*, 2018) and wind, as well as the electric vehicles, fed by battery, connected in the low and medium-voltage networks (PUTRUS *et al.*, 2009; RODRIGUES *et al.*, 2013).

Although the balancing of single- and two-phases electric loads between the distribution feeders can contribute to minimize these undesired effects it may not be sufficient to comply to the unbalance guidelines. In this manner, the over-sizing of conductors and equipment to produce smaller voltage drops and to process higher currents are some of the actions taken by utilities and consumers to mitigate the undesirable effects of excessive voltage imbalances in the distribution networks. Another alternatives are the use of voltage regulators and tap-changing transformers (YAN *et al.*, 2018) and the connection of shunt-inductors to the less-charged phases or series-capacitors with the distribution feeders (MILLER, 1982).

Notwithstanding the above alternatives, there are several examples of successful

power electronic converters applications in electric networks for voltage control, harmonic filtering and reactive power compensation (ABUD *et al.*, 2017; CHIRAPONGSANANURAK *et al.*, 2012). In (WANG *et al.*, 2012) the authors propose the use of three-phase inverters that operate as interface circuits of distributed sources to compensate for distribution networks negative-sequence voltage imbalances. The use of three-phase four-wire VSCs allows also to compensate unbalanced currents where each phase current can be independently controlled (Long *et al.*, 2020).

There are also several papers in which the authors address the unbalanced operation of multilevel converters in applications such as APF and HVDC transmission systems (LI *et al.*, 2018). The design of positive- and negative-sequence current controllers for a High-Voltage Direct Current transmission system based on Modular Multilevel Converter (MMC-HVDC) is presented in (PRIETO-ARAUJO *et al.*, 2017). The proposed controllers ensure the stable operation of the converter even during severe voltage sags in the AC network. However, the performance of the controllers in the presence of zero-sequence unbalances was not investigated. In (LI *et al.*, 2017) an Active Power Filter based on Modular Multilevel Converter (MMC-APF) is connected to a network with unbalanced voltages. Two controllers regulate the positive- and negative-sequence currents synthesized by the converter. However, the MMC-APF does not correctly operate when the mains voltage presents zero-sequence imbalance.

In (BEHROUZIAN; BONGIORNO, 2017; OGHORADA; ZHANG, 2018) the authors investigate the capacity of a multilevel DSTATCOM based on cascade H-bridge connection to synthesize negative-sequence currents at its terminals. Two connection configurations were tested for the DSTATCOM (delta and star). Similar analysis was performed in (CUPERTINO *et al.*, 2018a) however for a DSTATCOM based on a MMC in Double-Star Chopper Cell (DSCC) and Single-Delta Bridge Cell (SDBC) configuration. Again, in the aforementioned works, the capacity of the DSTATCOM in performing zero-sequence compensation is not addressed.

During a fault, the voltages of the electric network become unbalanced and may compromise the operation of grid-connected converters. Thus, in (TSOLARIDIS *et al.*, 2016) the performance of a MMC-STATCOM is investigated during single-phase faults in the electric network. However, only negative-sequence imbalances were evaluated.

In (XU *et al.*, 2016) a MMC-STATCOM is connected to a medium voltage distribution network to regulate the positive-sequence voltage and to compensate for negative-sequence voltage unbalance at the PCC. However, this work does not deals with zero-sequence voltage compensation. Moreover, as in the aforementioned papers, no mathematical models are presented for the positive- and negative-sequence voltage control at the PCC. The lack of these models makes difficult the use of a mathematical methodology to design the gains of the AC voltage controllers.

Therefore, another objective of this thesis is to present positive-, negative- and zero-sequence network voltage compensation strategies in distribution networks by using the MMC-STATCOM. For the sake of organization of this thesis the zero-sequence voltage compensation will be presented in Chapter 4 while the positive- and negative-sequence voltage compensation will be presented in this chapter. Mathematical modellings, in the synchronous reference frame, will be presented and used to derive the positive- and negative-sequence control loops and to design the controller gains of the static compensator. The MMC-STATCOM will be controlled to synthesize currents at its terminals in order to regulate the positive-sequence voltage at the nominal value and to compensate the negative-sequence voltage imbalance at the PCC. Results of digital simulations of the MMC-STATCOM connected to a medium-voltage unbalanced distribution network will be used to demonstrate the network voltage compensation strategy.

3.2 THE POSITIVE- AND NEGATIVE-SEQUENCE NETWORK VOLTAGE COMPENSATION

This section presents the mathematical modellings to derive the positive- and negative-sequence current and voltage control loops for the MMC-STATCOM to regulate the positive-sequence voltage and to compensate the negative-sequence voltage at the PCC. Moreover, the control loops to regulate the DC terminal voltage and to compensate the circulating currents of the MMC-STATCOM are also presented. Digital simulation results are shown to demonstrate the network voltage compensation using the MMC-STATCOM.

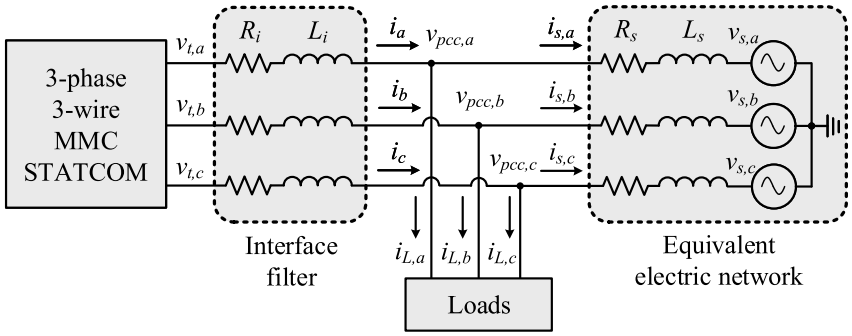
Diagram 13 shows the three-phase three-wire MMC-STATCOM connected to a distribution network through three first-order low-pass passive filter (L_i,R_i). These filters work as interface circuit between the converter and the mains terminals, minimizing the harmonic content of the MMC-STATCOM output currents. The equivalent electric network is modelled by the resistance R_s and the inductance L_s series-connected to an ideal three-phase source. The topology of the three-phase three-wire MMC-STATCOM is the same shown in Diagram 2.

In this chapter it is considered that the network voltages are unbalanced in such a way to present only positive- and negative-sequence components. Thus, the MMC-STATCOM should synthesize positive- and negative-sequence currents at its AC terminals in order to regulate the voltages at the PCC. However, before the measured voltages and currents be sent to the converter's controller, its positive- and negative-sequence components must be separated, as presented in the next section.

3.2.1 **The calculation of the positive- and negative-sequence components**

The separation, in the time domain, of the negative- and positive-sequence components of the voltages measured at the AC-side of the MMC-STATCOM starts applying

Diagram 13 – 3-phase 3-wire MMC-STATCOM connected to an equivalent electric network and loads.



Source: Elaborated by the author (2021).

the Clarke transform, as follows:

$$\begin{bmatrix} v_{pcc,\alpha} \\ v_{pcc,\beta} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{pcc,a} \\ v_{pcc,b} \\ v_{pcc,c} \end{bmatrix}, \tag{3.1}$$

where the zero-sequence component was omitted, since this chapter deals with only positive- and negative-sequence components.

The signals $v_{pcc,\alpha}$ and $v_{pcc,\beta}$ resulting from (3.1) feed the algorithm shown in Diagram 14. In this figure, two SOGIs (RODRIGUEZ *et al.*, 2006), similar to that shown in Diagram 15, are used to obtain the signals $v'_{pcc,\alpha}$, $qv'_{pcc,\alpha}$, $v'_{pcc,\beta}$ and $qv'_{pcc,\beta}$ that are combined to calculate the positive- and negative-sequence components.

In the last part of the Diagram 14, the positive- and negative-sequence voltages, in the $\alpha\beta$-coordinates, are transformed to the dq-coordinates, as follows:

$$\begin{bmatrix} v_{pcc,d1} \\ v_{pcc,q1} \end{bmatrix} = \begin{bmatrix} \cos(\rho) & \sin(\rho) \\ -\sin(\rho) & \cos(\rho) \end{bmatrix} \begin{bmatrix} v_{pcc,\alpha 1} \\ v_{pcc,\beta 1} \end{bmatrix} \tag{3.2}$$

and

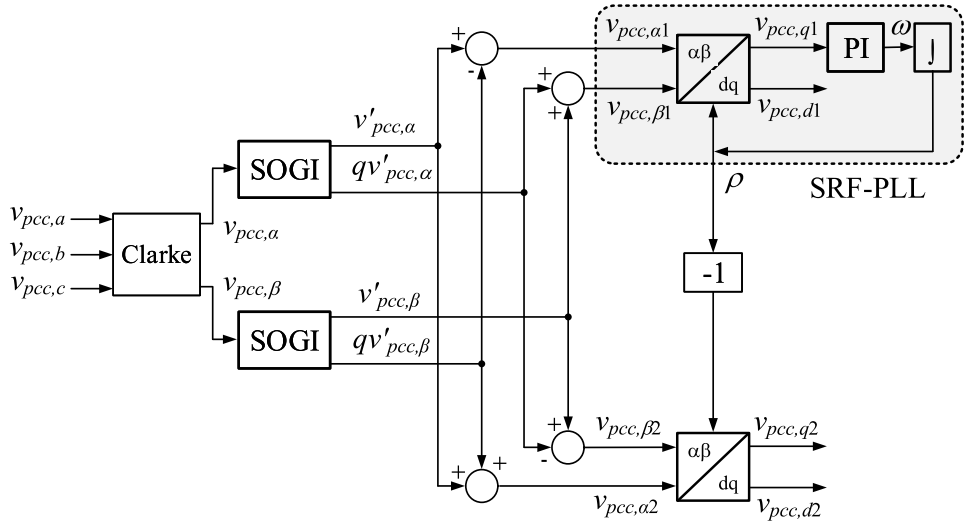
$$\begin{bmatrix} v_{pcc,d2} \\ v_{pcc,q2} \end{bmatrix} = \begin{bmatrix} \cos(-\rho) & \sin(-\rho) \\ -\sin(-\rho) & \cos(-\rho) \end{bmatrix} \begin{bmatrix} v_{pcc,\alpha 2} \\ v_{pcc,\beta 2} \end{bmatrix}, \tag{3.3}$$

where $d\rho/dt = \omega$ is the frequency tracked by the Phase-Locked Loop based on Synchronous Reference Frame (SRF-PLL).

In this thesis, the calculation of the positive- and negative-sequence current components is performed with the help of a notch filter instead of the SOGI circuit.

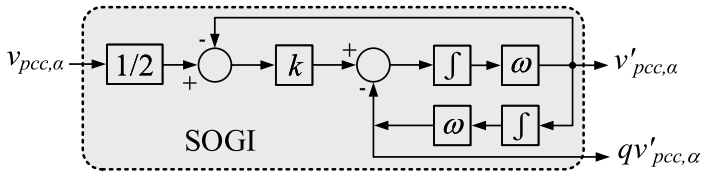
Diagram 16 shows the positive- and negative-sequence current detector. The MMC-STATCOM currents are measured and transformed to the $\alpha\beta$-coordinates in the

Diagram 14 – Block diagram for the positive- and negative-sequence voltage detector.



Source: Elaborated by the author (2021).

Diagram 15 – Block diagram for the SOGI.



Source: Elaborated by the author (2021).

same way the voltages are transformed in (3.1). The resulting currents are then transformed to the dq-coordinates by (3.2) and (3.3) and its oscillating parcels are eliminated by a notch filter, whose transfer function is given by:

$$F_n(s) = \frac{s^2 + \omega_o^2}{s^2 + \left(\frac{\omega_o}{Q}\right) s + \omega_o^2}, \tag{3.4}$$

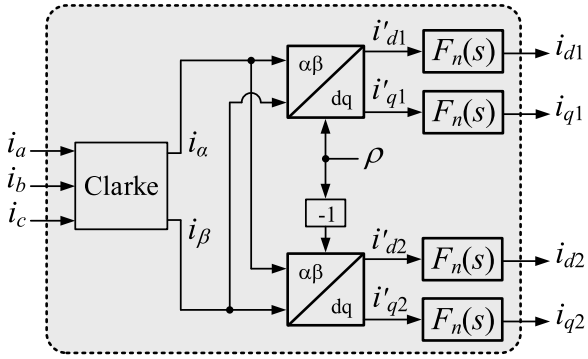
where Q and $\omega_o = 2\omega$ are the quality factor and the resonant frequency of the filter, $\omega = 2\pi f$ and f is the fundamental frequency of the electric network. Further details on the steps of the algorithm described in this section can be found in (ALMEIDA, 2011).

3.2.2 The positive- and negative-sequence current control loops

Neglecting the switching harmonics generated by the MMC-STATCOM, which are outside the spectrum of interest, the mathematical modelling of the circuit of Diagram 13, in the synchronous reference frame, allows to write the following equations for the converter's terminal positive-sequence currents:

$$L_{eq}\frac{di_{d1}}{dt} = +\omega L_{eq} i_{q1} - R_{eq} i_{d1} + v_{t,d1} - v_{pcc,d1} \tag{3.5}$$

Diagram 16 – Block diagram for the positive- and negative-sequence current detector.



Source: Elaborated by the author (2021).

and

$$L_{eq}\frac{di_{q1}}{dt} = -\omega L_{eq} i_{d1} - R_{eq} i_{q1} + v_{t,q1} - v_{pcc,q1}, \tag{3.6}$$

where i_{d1} and i_{q1} are the direct- and quadrature-axis terminal currents of the MMC-STATCOM, $v_{pcc,d1}$ e $v_{pcc,q1}$ are the voltages at the PCC, $L_{eq} = (L_i + L_f/2)$ and $R_{eq} = (R_i + R_f/2)$ are the equivalent inductance and resistance, respectively, $v_{t,d1} = m_{d1}(\frac{V_{dc}}{2})$ and $v_{t,q1} = m_{q1}(\frac{V_{dc}}{2})$ are the MMC-STATCOM terminal voltages, being V_{dc} the DC terminal voltage, m_d and m_q the converter's modulation indexes, $\omega = (2\pi f)$ the angular frequency of the voltages at the PCC and the subscript $(_1)$ indicating the positive-sequence.

Introducing the new control variables u_{d1} and u_{q1} in (3.5) and (3.6), the terminal voltages of the MMC-STATCOM are given by:

$$v_{t,d1} = -\omega L_{eq} i_{q1} + v_{pcc,d1} + u_{d1} \tag{3.7}$$

and

$$v_{t,q1} = +\omega L_{eq} i_{d1} + v_{pcc,q1} + u_{q1}. \tag{3.8}$$

Replacing (3.7) and (3.8) into (3.5) and (3.6), respectively, yields the following first-order dynamic system:

$$L_{eq}\frac{di_{d1}}{dt} = -R_{eq} i_{d1} + u_{d1} \tag{3.9}$$

$$L_{eq}\frac{di_{q1}}{dt} = -R_{eq} i_{q1} + u_{q1}. \tag{3.10}$$

Besides the variables $v_{pcc,d1}$ and $v_{pcc,q1}$ mitigate the influence of the grid voltage on the currents synthesized by the MMC-STATCOM, the cross-coupling between the direct- and quadrature-axis currents are eliminated. Since the dynamic behaviour of the system given by (3.9) and (3.10) is decoupled, the currents i_{d1} and i_{q1} can be regulated by PI

controllers, as shown bellow:

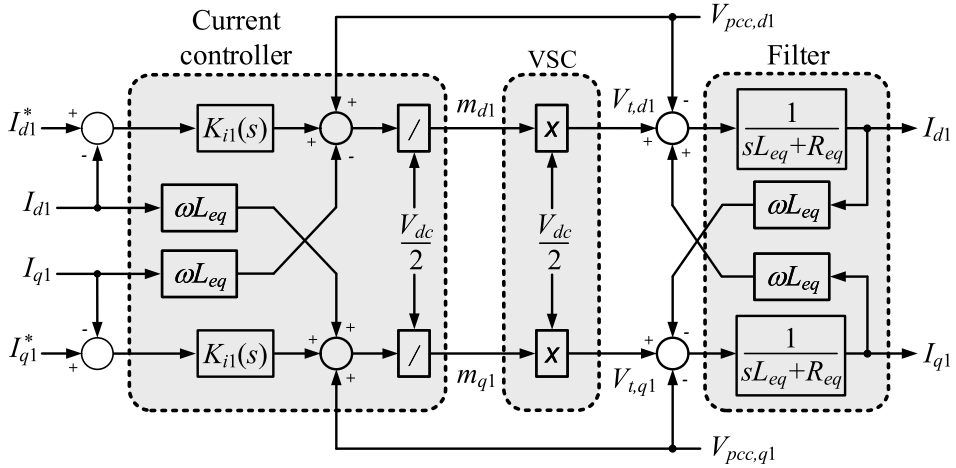
$$u_{d1} = k_{p1}\varepsilon_{d1} + k_{i1}\int_{-\infty}^{t} \varepsilon_{d1} d\lambda \tag{3.11}$$

$$u_{q1} = k_{p1}\varepsilon_{q1} + k_{i1}\int_{-\infty}^{t} \varepsilon_{q1} d\lambda, \tag{3.12}$$

where $\varepsilon_{d1} = (i^*_{d1} - i_{d1})$ and $\varepsilon_{q1} = (i^*_{q1} - i_{q1})$ are the errors between the reference currents (i^*_{d1}, i^*_{q1}) and the MMC-STATCOM currents (i_{d1}, i_{q1}), respectively; k_{p1} and k_{i1} are the proportional and integral gains of the current regulators, respectively, and λ is a dummy variable.

Diagram 17 shows the block diagram of the direct- and quadrature-axis positive-sequence current control loops. From (3.9)–(3.12), the gains of the controller $K_{i1}(s)$ can be chosen equal to $k_{p,i1} = (L_{eq}/\tau_{i1})$ and $k_{i,i1} = (R_{eq}/\tau_{i1})$ to ensure a first-order response to the closed-loop transfer function, where τ_{i1} is the desired time constant (ALMEIDA *et al.*, 2016; FOGLI; ALMEIDA; BARBOSA, 2017; YAZDANI; IRAVANI, 2010).

Diagram 17 – Block diagram for the direct- and quadrature-axis positive-sequence current control loops.

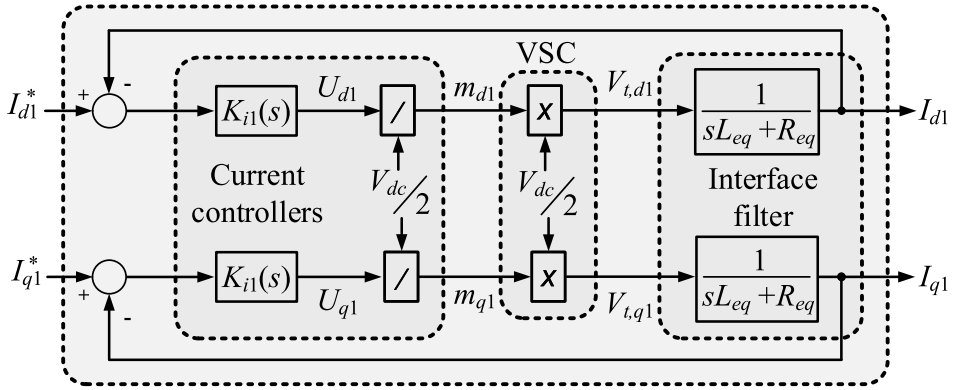


Source: Elaborated by the author (2021).

Due to the adding of the current decoupling and the feed-forward signals the Diagram 17 can be simplified, as shown in Diagram 18, where the cross-coupling signals and the feed-forward voltages were omitted.

The same design steps can be used to regulate the negative-sequence currents, however with the synchronous reference frame rotating in the clockwise direction. Diagram 19 shows the block diagram of the control loop used to regulate the currents I_{d2} and I_{q2}. The subscript ($_2$) is used to identify the new controllers $K_{i2}(s)$ and variables. In this figure, the design of loops to compensate the cross-coupling between the negative-sequence currents and the effect of the PCC voltages, makes it possible to redraw this block diagram as that one shown in Diagram 18. However, it can be noted in Diagram 19

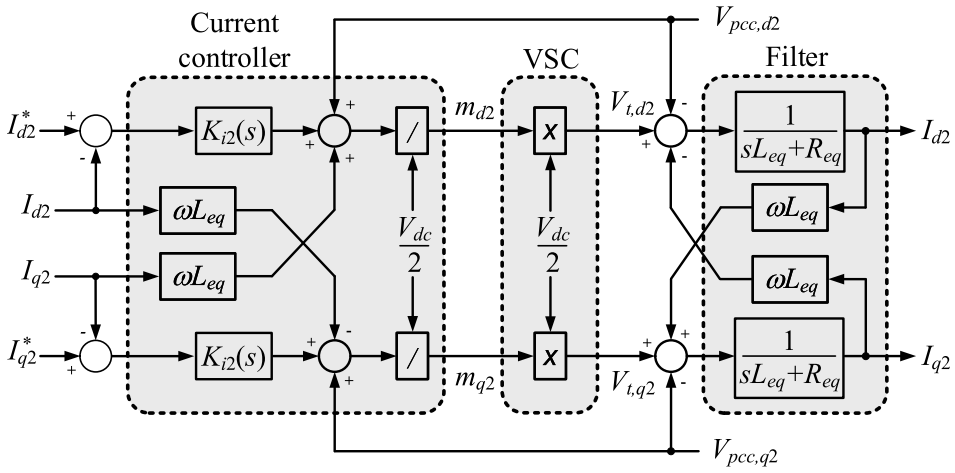
Diagram 18 – Simplified block diagram for the direct- and quadrature-axis positive-sequence current control loops.



Source: Elaborated by the author (2021).

that the cross-coupling between the negative-sequence currents have inverted signs compared to the positive-sequence ones. The gains of the negative-sequence current controller $K_{i2}(s) = (k_{p,i2} + k_{i,i2}/s)$ can be chosen equal to $k_{p,i2} = (L_{eq}/\tau_{i2})$ and $k_{i,i2} = (R_{eq}/\tau_{i2})$, where τ_{i2} is the desired time constant.

Diagram 19 – Block diagram for the direct- and quadrature-axis negative-sequence current control loops.



Source: Elaborated by the author (2021).

3.2.3 **The positive-sequence voltage control loop**

Considering the electric network of Diagram 13 as reference, the following equations for the positive-sequence voltages at the PCC can be written:

$$v_{pcc,d1} = L_{s1}\frac{di_{s,d1}}{dt} - \omega L_{s1} i_{s,q1} + R_{s1} i_{s,d1} + v_{s,d1} \tag{3.13}$$

and

$$v_{pcc,q1} = L_{s1}\frac{di_{s,q1}}{dt} + \omega L_{s1} i_{s,d1} + R_{s1} i_{s,q1} + v_{s,q1}, \tag{3.14}$$

where R_{s1} and L_{s1} are the positive-sequence resistance and inductance of the electric network, respectively; $v_{s,d1} = \hat{V}_{s1}\cos(\omega_s t + \phi_{s1} - \rho)$ and $v_{s,q1} = \hat{V}_{s1}\sin(\omega_s t + \phi_{s1} - \rho)$; $\hat{V}_{s1}$, ω_s and ϕ_{s1} are the peak value, the angular frequency and the phase of the positive-sequence voltage of the network, respectively.

The linearisation of (3.13) and (3.14) results in the following small-signal model for the MMC-STATCOM:

$$\bar{V}_{pcc,d1} = -\bar{\omega} L_{s1}\bar{I}_{s,q1} + R_{s1}\bar{I}_{s,d1} + \hat{V}_s\cos\bar{\rho}_0 \tag{3.15}$$

$$\bar{V}_{pcc,q1} = +\bar{\omega} L_{s1}\bar{I}_{s,d1} + R_{s1}\bar{I}_{s,q1} - \hat{V}_s\sin\bar{\rho}_0 \tag{3.16}$$

and

$$\tilde{v}_{pcc,d1} = L_{s1}\frac{d\tilde{i}_{s,d1}}{dt} - \tilde{\omega} L_{s1}\bar{I}_{s,q1} - \bar{\omega} L_{s1}\tilde{i}_{s,q1} + R_{s1}\tilde{i}_{s,d1} - (\hat{V}_s\sin\bar{\rho}_0)\tilde{\rho} \tag{3.17}$$

$$\tilde{v}_{pcc,q1} = L_{s1}\frac{d\tilde{i}_{s,q1}}{dt} + \tilde{\omega} L_{s1}\bar{I}_{s,d1} + \bar{\omega} L_{s1}\tilde{i}_{s,d1} + R_{s1}\tilde{i}_{s,q1} - (\hat{V}_s\cos\bar{\rho}_0)\tilde{\rho}, \tag{3.18}$$

where $\cos(\omega_s t + \phi_{s1} - \rho) \approx \cos(\bar{\rho}_0 + \tilde{\rho}) \approx \cos\bar{\rho}_0 - (\sin\bar{\rho}_0)\tilde{\rho}$ and $\sin(\omega_s t + \phi_{s1} - \rho) \approx -\sin(\bar{\rho}_0 + \tilde{\rho}) \approx -\sin\bar{\rho}_0 - (\cos\bar{\rho}_0)\tilde{\rho}$, considering $\tilde{\rho} << 1$.

The voltages, currents and angles in (3.15)–(3.18) with the symbol ($\bar{}$) represent the steady-state while the ones highlighted with the symbol ($\tilde{}$) represent the small disturbances around the operating point.

Considering also the small signal model of the PLL, the following additional equation can be written:

$$\frac{d\tilde{\rho}}{dt} = h\,(p)\,\tilde{v}_{pcc,q1}, \tag{3.19}$$

where $p = d(\cdot)/dt$ is the differential operator and $h\,(p)$ is the zero-state response of the transfer function $H\,(s)$ of the PLL.

Considering $\bar{V}_{pcc,q1} = 0$, $\tilde{\rho} << 1$ and $\bar{V}_{pcc,d1} >> \tilde{v}_{pcc,d1}$, the following relation can be written:

$$\tilde{v}_{pcc,q1} = \bar{V}_{pcc,d1}\tilde{\rho}. \tag{3.20}$$

The substitution of (3.20) in (3.19) provides the following small-signal model for the PLL:

$$\frac{d\tilde{\rho}}{dt} = h\,(p)\,\bar{V}_{pcc,d1}\tilde{\rho}. \tag{3.21}$$

Solving simultaneously (3.15)–(3.18) and (3.21), considering that the PLL tracks the positive-sequence voltage with a null error in steady-state, the small-signal relation, in the frequency domain, for the direct-axis voltage at the PCC is given by:

$$\tilde{V}_{pcc,d1}(s) = G_{d1}(s)\tilde{I}_{s,d1}(s) - G_{q1}(s)\tilde{I}_{s,q1}(s), \tag{3.22}$$

where $G_{d1}(s) = (sL_{s1} + R_{s1})$ and $G_{q1}(s) = \bar{\omega}L_{s1}$.

Substituting the currents $\tilde{I}_{s,d1}(s)$ and $\tilde{I}_{s,q1}(s)$ in (3.22) by the difference between the currents synthesized by the MMC-STATCOM, $\tilde{I}_{d1}(s)$ and $\tilde{I}_{q1}(s)$, and the currents drained by the load, $\tilde{I}_{L,d1}(s)$ and $\tilde{I}_{L,q1}(s)$, (3.22) can be rewritten by:

$$\tilde{V}_{pcc,d1}(s) = -G_{d1}(s)\tilde{I}_{L,d1}(s) + G_{q1}(s)\tilde{I}_{L,q1}(s) + G_{d1}(s)\tilde{I}_{d1}(s) - G_{q1}(s)\tilde{I}_{q1}(s). \quad (3.23)$$

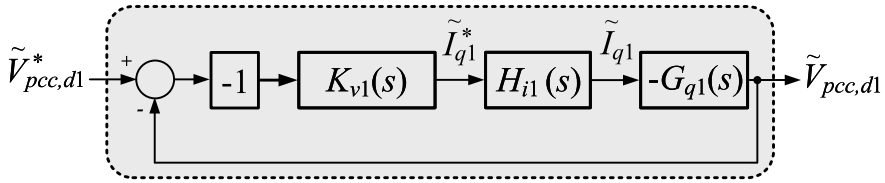
The analysis of the two first parcels of (3.23) shows that $\tilde{V}_{pcc,d1}(s)$ depends directly on the currents drained by the load. Moreover, this voltage can be controlled by the currents $\tilde{I}_{d1}(s)$ and $\tilde{I}_{q1}(s)$ synthesized by the MMC-STATCOM.

Since the X/R relation in distribution systems vary from 1.5 to 3 for low-voltage systems (near transformers) and 3 to 20 for medium-voltage systems (SALLAM; MALIK, 2018) and considering that $\tilde{I}_{d1} \approx 0$, since the MMC-STATCOM absorb a small amount of active power at its terminals to compensate its power losses, it is more interesting to control the voltage $\tilde{V}_{pcc,d1}$ using the current $\tilde{I}_{q1}$. Since the MMC-STATCOM should synthesize currents to regulate the voltages at the PCC, this strategy is suitable for distribution networks with low short-circuit power (high equivalent impedance), since the currents synthesized by the compensator will also be low.

Figure 42 (a) shows the phasor diagram for the mains voltage, the PCC voltage, the current through the network and the voltage-drops across the resistance and inductance of the network. It can be noted that the PLL ensures the voltage $V_{pcc,1}$ in the direction of the d-axis. Figure 42 (b) and Figure 42 (c) show the voltage drops presented in (3.15) and (3.16), on the direct- and quadrature-axis, respectively. It can be noted that the voltage drops $\omega L_{s1} I_{s,q1}$ and $\omega L_{s1} I_{s,d1}$ are on the direct- and quadrature-axis, respectively.

Diagram 20 shows the block diagram for the positive-sequence voltage control loop. The block $H_{i1}(s)$ represents the closed-loop transfer function of the positive-sequence current controller of Diagram 17 while $K_{v_1}(s)$ represents the positive-sequence voltage controller. The block with the unitary negative gain compensates the signal of the plant.

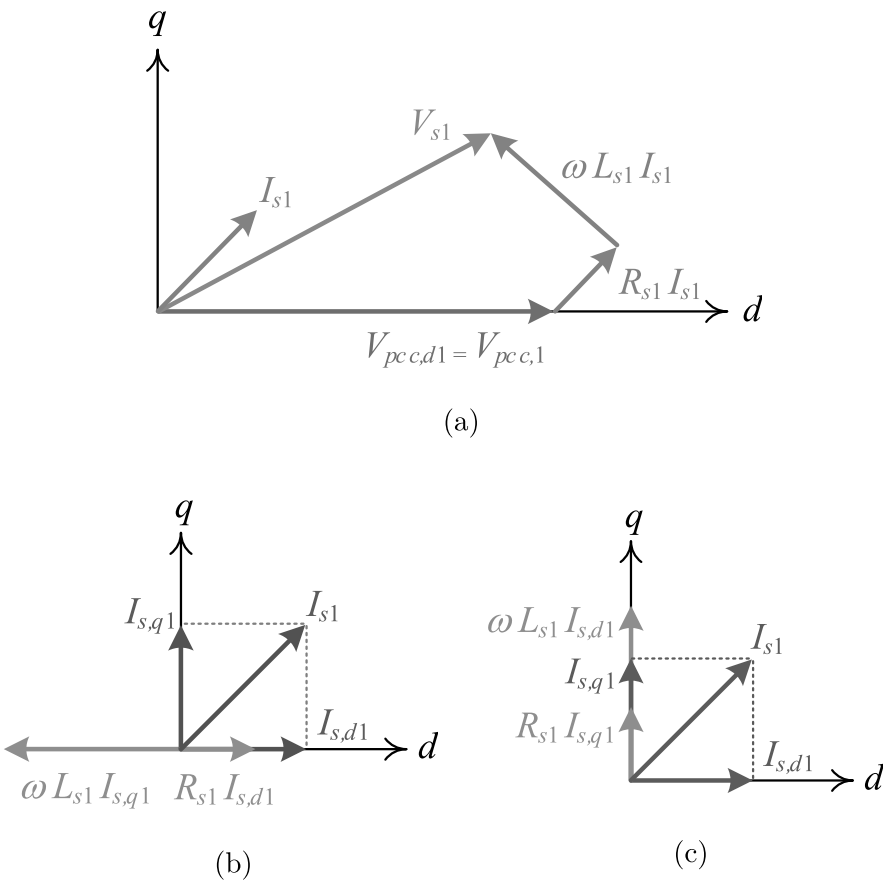
Diagram 20 – Block diagram for the direct-axis positive-sequence voltage control loop.



Source: Elaborated by the author (2021).

The controller $K_{v_1}(s)$ can be chosen of the integral type since $G_{q1}(s)$ was modelled by a constant gain in (3.23). Thus, it is assured that the output asymptotically tracks the input signal with a first-order dynamic and zero steady-state error. Assuming $H_{i1}(s) = 1$

Figure 42 – Phasor diagrams for the positive-sequence voltages and currents.



Caption: (a) complete phasor diagram, (b) voltage drops on the direct-axis and (c) voltage drops on the quadrature-axis.

Source: Elaborated by the author (2021).

and the time constant of the voltage controller $\tau_{v1} \geq (10\tau_{i1})$, the following closed-loop transfer function can be written for the Diagram 20:

$$H_{v1}(s) = \frac{1}{s\tau_{v1} + 1}, \tag{3.24}$$

where $\tau_{v1} = 1/(k_{v1}\bar{\omega}L_{s1})$ is the desired time constant and k_{v1} is the gain of the controller $K_{v1}(s) = k_{v1}/s$.

The same control strategy can be used to design the controllers to compensate for negative-sequence voltage unbalances on the network, as will be discussed in the next subsection.

3.2.4 The negative-sequence voltage control loops

Again, starting from the network-side terminals of Diagram 13, however considering the synchronous reference frame rotating in the clockwise direction, the following relations can be written in the dq-frame for the negative-sequence voltage at the PCC:

$$v_{pcc,d2} = L_{s2}\frac{di_{s,d2}}{dt} + \omega L_{s2} i_{s,q2} + R_{s2} i_{s,d2} + v_{s,d2} \tag{3.25}$$

and

$$v_{pcc,q2} = L_{s2}\frac{di_{s,q2}}{dt} - \omega L_{s2} i_{s,d2} + R_{s2} i_{s,q2} + v_{s,q2}, \tag{3.26}$$

where R_{s2} and L_{s2} are the negative-sequence resistance and inductance of the network, respectively; $v_{pcc,d2}$ and $v_{pcc,q2}$ are the negative-sequence voltages at the PCC; $v_{s,d2} = \hat{V}_{s2}\cos(\omega_s t + \phi_{s2} - \rho)$ and $v_{s,q2} = \hat{V}_{s2}\sin(\omega_s t + \phi_{s2} - \rho)$; $\hat{V}_{s2}$ and ϕ_{s2} are the peak value and the phase of the negative-sequence voltages of the network, respectively; $\rho = (\omega t + \phi)$ is the angle tracked by the PLL, where ω and ϕ are the fundamental angular frequency and phase angle of the positive-sequence voltage at the PCC, respectively.

The comparison of (3.25)–(3.26) and (3.13)–(3.14) allows to use the same steps presented in Subection 3.2.3 to obtain small-signal transfer functions for the negative-sequence voltages at the PCC, resulting in:

$$\tilde{V}_{pcc,d2}(s) = G_{d2}(s)\tilde{I}_{d2}(s) - G_{q2}(s)\tilde{I}_{q2}(s) - G_{d2}(s)\tilde{I}_{L,d2}(s) + G_{q2}(s)\tilde{I}_{L,q2}(s) \tag{3.27}$$

and

$$\tilde{V}_{pcc,q2}(s) = G_{d2}(s)\tilde{I}_{q2}(s) + G_{q2}(s)\tilde{I}_{d2}(s) - G_{d2}(s)\tilde{I}_{L,q2}(s) - G_{q2}(s)\tilde{I}_{L,d2}(s), \tag{3.28}$$

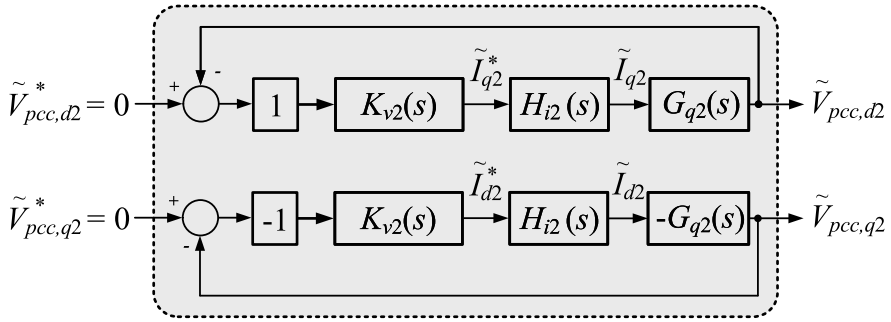
where $G_{d2}(s) = (R_{s2} + sL_{s2})$; $G_{q2}(s) = \bar{\omega}L_{s2}$; $\tilde{I}_{d2}(s)$ and $\tilde{I}_{q2}(s)$ are the direct- and quadrature-axis currents synthesized by the MMC-STATCOM, respectively; $\tilde{I}_{L,d2}(s)$ and $\tilde{I}_{L,q2}(s)$ are the direct- and quadrature-axis currents drained by the load, respectively.

The analysis of (3.27) and (3.28) shows that, although the voltages $\tilde{V}_{pcc,d2}(s)$ and $\tilde{V}_{pcc,q2}(s)$ depend on the currents drained by the load, they can be controlled by the currents $\tilde{I}_{d2}(s)$ and $\tilde{I}_{q2}(s)$ synthesized by the MMC-STATCOM.

Diagram 21 shows the block diagram for the negative-sequence voltage control loop. Different from the positive-sequence voltage control loop, two controllers are used, one for the direct-axis and another for the quadrature-axis. The current $\tilde{I}_{q2}(s)$ is used to control the voltage $\tilde{V}_{pcc,d2}(s)$, while the voltage $\tilde{V}_{pcc,q2}(s)$ is controlled by the current

$\tilde{I}_{d2}(s)$. The blocks $H_{i2}(s)$ and $K_{v2}(s)$ represent the closed-loop transfer function of the negative-sequence current control loop of Diagram 19 and the transfer function of the negative-sequence voltage controller, respectively.

Diagram 21 – Block diagram for the direct- and quadrature-axis negative-sequence voltage control loops.



Source: Elaborated by the author (2021).

Since the cross-coupling between the direct- and quadrature-axis currents in (3.13)–(3.14) and (3.25)–(3.26) have inverted signs, it can be noted that the plant $G_{q2}(s) = \bar{\omega}L_{s2}$ of the control loops of Diagram 21 have also inverted signs compared to the positive-sequence voltage control loop of Diagram 20.

If the negative-sequence current controller is designed so that the time constant of the transfer function H_{i2} is much smaller than the time constant of the negative-sequence voltage control loop, the transfer function $H_{i2}(s)$ can be considered an unitary gain and then the closed-loop transfer function of the negative-sequence voltage control loop is given by:

$$H_{v2}(s) = \frac{1}{s\tau_{v2} + 1}, \tag{3.29}$$

where $\tau_{v2} = 1/(k_{v2}\bar{\omega}L_{s2})$ is the time constant of the negative-sequence voltage control loop and k_{v2} is the gain of the integral controller $K_{v2}(s) = k_{v2}/s$. The gain k_{v2} of the controller $K_{v2}(s)$ can be calculated by choosing the desired time constant for $H_{v2}(s)$.

3.2.5 The DC voltage control of the MMC-STATCOM

The control of the MMC-STATCOM DC terminal voltage can be performed by forcing the converter to inject or drain positive-sequence currents from the grid. Then, the mathematical modelling of the MMC-STATCOM DC-side voltage dynamics, in the synchronous reference frame, can be performed by applying a power balance (ALMEIDA *et al.*, 2016) between the converter's AC- and DC-side, yielding the following differential equation:

$$\frac{dV_{dc}^2}{dt} = P_c\cos(2\omega t) + P_s\sin(2\omega t) - \frac{3L_{eq}}{2C_{eq}}\left(\frac{di_{d1}^2}{dt} + \frac{di_{q1}^2}{dt} + \frac{di_{d2}^2}{dt} + \frac{di_{q2}^2}{dt}\right) -$$
$$-\frac{3R_{eq}}{C_{eq}}\left(i_{d1}^2 + i_{q1}^2 + i_{d2}^2 + i_{q2}^2\right) - \frac{3}{C_{eq}}\left(v_{pcc,d1}i_{d1} + v_{pcc,q1}i_{q1} + v_{pcc,d2}i_{d2} + v_{pcc,q2}i_{q2}\right) \quad (3.30)$$

where,

$$P_c = -3\left\{\left(v_{pcc,d1}i_{d2} + v_{pcc,q1}i_{q2} + v_{pcc,d2}i_{d1} + v_{pcc,q2}i_{q1}\right) + \right.$$
$$\left. +2\omega L_{eq}\left(i_{d1}i_{q2} - i_{q1}i_{d2}\right) + 2R_{eq}\left(i_{d1}i_{d2} + i_{q1}i_{q2}\right)\right\}/C_{eq} \quad (3.31)$$

and,

$$P_s = -3\left\{\left(v_{pcc,q2}i_{d1} - v_{pcc,d2}i_{q1} - v_{pcc,q1}i_{d2} + v_{pcc,d1}i_{q2}\right) - \right.$$
$$\left. -2\omega L_{eq}\left(i_{d1}i_{d2} + i_{q1}i_{q2}\right) + 2R_{eq}\left(i_{d1}i_{q2} - i_{q1}i_{d2}\right)\right\}/C_{eq}. \quad (3.32)$$

In (ALMEIDA *et al.*, 2016) is shown that the average parcel of V_{dc}^2 can be controlled by the direct-axis positive-sequence current. After applying the Laplace transform and performing a small-signal linearisation in (3.30), the following simplified transfer function can be written:

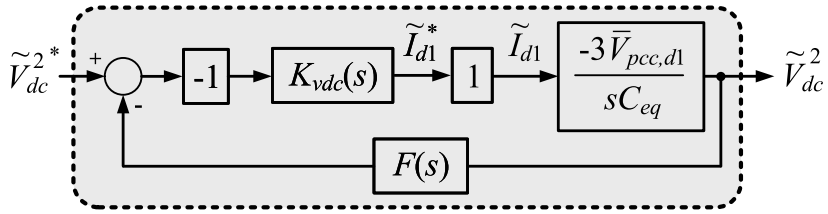
$$\frac{\tilde{y}_0(s)}{\tilde{I}_{d1}(s)} = \frac{-3\bar{V}_{pcc,d1}}{sC_{eq}}, \quad (3.33)$$

where $\tilde{y}_0$ is the small-signal average parcel of V_{dc}^2 and $\bar{V}_{pcc,d1}$ is the steady-state value of the direct-axis positive-sequence voltage at the PCC.

Diagram 22 shows the block diagram of the DC voltage control loop. The error from the comparison between the reference value $(V_{dc}^*)^2$ and V_{dc}^2 feeds the PI-controller $K_{vdc}(s)$ which output is the reference current I_{d1}^*. The block with the negative unitary gain compensates the signal of the transfer function of the plant. A first-order low-pass filter $F(s)$ was connected to the feedback path to filter the signal measured at the DC terminals of the MMC-STATCOM.

Assuming the time constant of the DC voltage closed-loop at least one decade higher than the time constant of the direct-axis positive-sequence current closed-loop, one can make $H_{i1}(s) = 1$, resulting in the following closed-loop transfer function for the

Diagram 22 – Block diagram for the DC voltage control loop of the MMC-STATCOM.



Source: Elaborated by the author (2021).

Diagram 22:

$$H_{vdc}(s) = \frac{s^2\left(\frac{3k_{p,vdc}\bar{V}_{pcc,d1}}{C_{eq}}\right) + s\left(\frac{3k_{i,vdc}\bar{V}_{pcc,d1} + 3k_{p,vdc}\bar{V}_{pcc,d1}\omega_0}{C_{eq}}\right) + \frac{3k_{i,vdc}\bar{V}_{pcc,d1}\omega_0}{C_{eq}}}{s^3 + s^2\omega_0 + s\left(\frac{3k_{p,vdc}\bar{V}_{pcc,d1}\omega_0}{C_{eq}}\right) + \frac{3k_{i,vdc}\bar{V}_{pcc,d1}\omega_0}{C_{eq}}}, \tag{3.34}$$

where $k_{p,vdc}$ and $k_{i,vdc}$ are the proportional and integral gains of the DC voltage regulator $K_{vdc}(s) = k_{p,vdc} + k_{i,vdc}/s$.

The proportional and integral gains of $K_{vdc}(s)$ can be calculated by comparing the denominator of (3.34) to the third-order characteristic polynomial $P(s) = (s^3 + 2\omega_n s^2 + 2\omega_n^2 s + \omega_n^3)$ (ÅSTRÖM; WITTENMARK, 2013) as given bellow:

$$k_{p,vdc} = \frac{C_{eq}\omega_0}{6\bar{V}_{pcc,d1}} \tag{3.35}$$

and

$$k_{i,vdc} = \frac{C_{eq}\omega_0^2}{24\bar{V}_{pcc,d1}}, \tag{3.36}$$

where $\omega_n = \omega_0/2$ and ω_0 is the cut-off frequency of the low-pass filter $F(s)$.

3.2.6 **The circulating currents compensation**

As discussed in Subection 1.2.4 it is important to compensate the circulating currents of the MMC. The upper and lower arm currents of the three-phase three-wire MMC are formed by three components: AC component at the fundamental frequency, DC component responsible by the power transfer between the AC- and DC-side of the converter and circulating current as follows:

$$i_{upp,k} = -\frac{i_k}{2} + \frac{i_{dc}}{3} + i_{cir,k} \tag{3.37}$$

$$i_{lwr,k} = +\frac{i_k}{2} + \frac{i_{dc}}{3} + i_{cir,k} \tag{3.38}$$

where i_k is the phase-current of the MMC, i_{dc} is the current of the DC-link, i_{cir} is the circulating current (mainly composed by negative-sequence second-harmonic component) and $k = \{a, b, c\}$ is the phase of the converter (ALMEIDA, 2019; GHETTI, 2019).

In applications such as the STATCOM, the DC current is null. Thus, according to (3.37) and (3.38) the circulating current can be calculated by:

$$i_{cir,k} = \frac{i_{upp,k} + i_{lwr,k}}{2}. \tag{3.39}$$

Analysing the circuit of one phase of the MMC of Diagram 1, the dynamic of the circulating current is given by:

$$L_f \frac{di_{cir,k}}{dt} + R_f i_{cir,k} = \left(\frac{V_{dc}}{2}\right) - \left(\frac{u_{upp,k} + u_{lwr,k}}{2}\right), \tag{3.40}$$

where $u_{upp,k}$ and $u_{lwr,k}$ represent the voltages of the upper and lower arms.

In (3.40) it is possible to note that the circulating currents can be mitigated controlling the imbalance branch voltages given by:

$$v_{im,k} = L_f \frac{di_{cir,k}}{dt} + R_f i_{cir,k}. \tag{3.41}$$

Manipulating (3.40) and (3.41) the new reference voltages for the arms of the MMC are given by:

$$v^*_{upp,k} = \frac{V_{dc}}{2} - v^*_k - v^*_{im,k} \tag{3.42}$$

and

$$v^*_{lwr,k} = \frac{V_{dc}}{2} + v^*_k - v^*_{im,k}, \tag{3.43}$$

where v^*_k is the reference for the terminal voltage of the MMC.

The relations (3.42) and (3.43) are normalized in order to be used in the multi-carrier PWM. Then, the normalized modulation indexes for the MMC's upper and lower arms are given by:

$$m_{upp,k} = 0.5\,(1 - m_k) - m_{im,k} \tag{3.44}$$

and

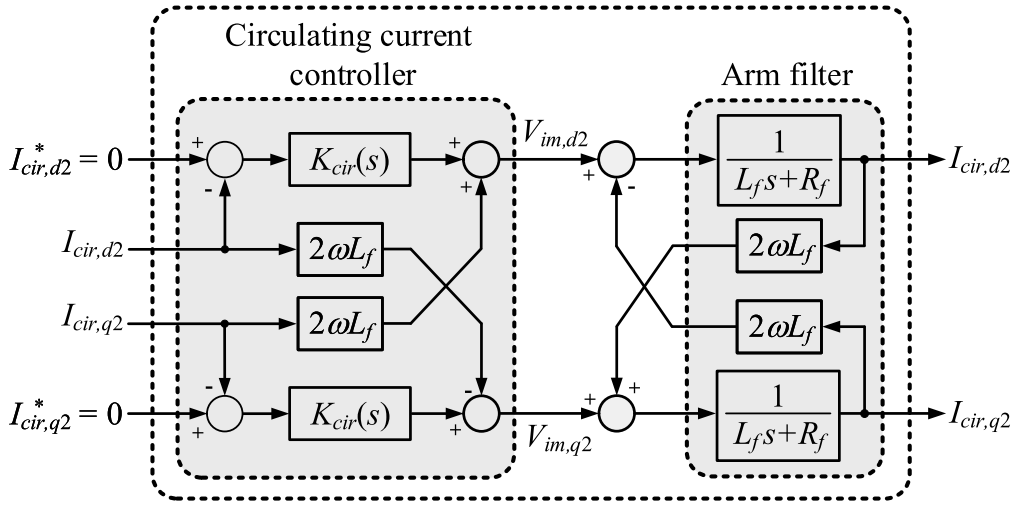
$$m_{lwr,k} = 0.5\,(1 + m_k) - m_{im,k}, \tag{3.45}$$

where $m_{upp,k} = (v^*_{upp,k}/V_{dc})$, $m_{lwr,k} = (v^*_{lwr,k}/V_{dc})$ and $m_{im,k} = (v^*_{im,k}/V_{dc})$ (ALMEIDA, 2019; ALMEIDA *et al.*, 2017; GHETTI, 2019).

The control strategy used in this work is based on the transformation of the circulating currents into the synchronous reference frame rotating at twice the fundamental frequency (DU *et al.*, 2018; ALMEIDA *et al.*, 2017; TU; XU; XU, 2011). In this new

reference frame, the second-harmonic circulating currents assume a stationary characteristic and can be easily controlled using PI regulators as shown in the Diagram 23.

Diagram 23 – Block diagram for the second harmonic circulating current control loop.



Source: Elaborated by the author (2021).

Assuming the cross-coupling between the direct- and quadrature-axis circulating currents components is fully compensated, the following closed-loop transfer function can be written (ALMEIDA *et al.*, 2017):

$$H_{i2,cir}(s) = \frac{\left(\frac{k_{p,cir}}{L_f}\right)s + \frac{k_{i,cir}}{L_f}}{s^2 + \left(\frac{k_{p,cir} + R_f}{L_f}\right)s + \frac{k_{i,cir}}{L_f}}, \tag{3.46}$$

where $k_{p,cir}$ and $k_{i,cir}$ are the proportional and integral gains of the circulating current controller $K_{cir}(s) = k_{p,cir} + k_{i,cir}/s$, respectively.

The gains of $K_{cir}(s)$ can be designed by comparing the denominator of (3.46) to the second-order canonic transfer function $H(s) = (s^2 + 2\zeta\omega_n s + \omega_n^2)$, resulting in:

$$k_{p,cir} = 2\zeta\omega_n L_f - R_f \tag{3.47}$$

and

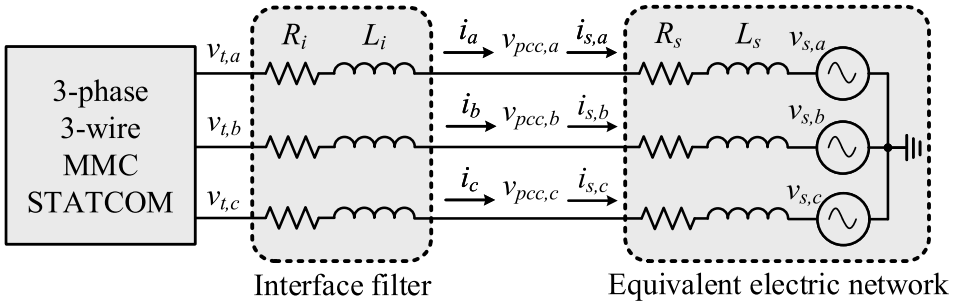
$$k_{i,cir} = L_f\omega_n^2. \tag{3.48}$$

3.3 DIGITAL SIMULATION OF THE POSITIVE- AND NEGATIVE-SEQUENCE VOLTAGE COMPENSATION STRATEGY

Diagram 24 shows the static compensator connected to a distribution network. The circuit of Diagram 24 and the three-phase three-wire MMC-STATCOM, similar to that shown in Diagram 2, with all its controllers were modelled in an electromagnetic transient

program in order to demonstrate the compensation of the PCC voltages. Tables 8, 9, 10 and 4 show the parameters of the electric network, MMC-STATCOM, digital filters and controllers, respectively. Each leg of the MMC-STATCOM was modelled with twenty eight SMs connected in series, fourteen SMs in the upper and fourteen SMs in the lower arm. However, in high-voltage applications, the number of SMs per converter arm can reach hundreds of units (DU *et al.*, 2018).

Diagram 24 – 3-phase 3-wire MMC-STATCOM connected to an equivalent electric network.



Source: Elaborated by the author (2021).

Table 4 – Controller gains of the 3-phase 3-wire MMC-STATCOM with 14 SMs per leg.

Controller	**Gain**	**Value**
$K_{i1}(s)$	$k_{p,i1}$	31.6 V/A
	$k_{i,i1}$	0.5 kV/(A s)
$K_{v1}(s)$	k_{v1}	40.3 A/(V s)
$K_{i2}(s)$	$k_{p,i2}$	31.6 V/A
	$k_{i,i2}$	0.5 kV/(A s)
$K_{v2}(s)$	k_{v2}	40.3 A/(V s)
$K_{vdc}(s)$	$k_{p,vdc}$	12.2 µA/V^2
	$k_{i,vdc}$	1.22 µA/(V^2 s)
$K_{cir}(s)$	$k_{p,cir}$	6.07 V/A
	$k_{i,cir}$	632 V/(A s)

Source: Elaborated by the author (2021).

All controllers of the MMC-STATCOM were implemented digitally. They were discretized using the bilinear approximation, considering a sampling frequency equal to 25 kHz. Since the sampling frequency is ten times greater than the bandwidth of the controllers, the distortion of the output signals caused by the discretization of the controllers will be less than 3% (BUSO; MATTAVELLI, 2015).

The switching patterns for the IGBTs of the MMC-STATCOM are generated using a PD-PWM technique. The SM DC capacitors voltages of the static compensator are regulated using an algorithm that measures and sorts the SMs in descending order according to their DC voltages, as proposed in (GHETTI *et al.*, 2017), while the DC

terminal voltage of the MMC-STATCOM is regulated by using the DC voltage control loop of Diagram 22.

Three cases will be investigated: (*i*) positive-sequence voltage regulation, (*ii*) negative-sequence voltage compensation and (*iii*) both strategies working simultaneously. In all cases the circulating current control is active, however, this topic will be presented only in the next chapter, for the three-phase four-wire MMC-STATCOM, in order to avoid redundancies. The imbalance in the PCC voltages was simulated by connecting three voltage sources in series, for the positive-, negative- and zero-sequence components, with each phase of the ending-side of the network. This scheme will allow testing the MMC-STATCOM's ability to compensate for voltages at the PCC when the grid is unbalanced. Table 5 shows the RMS values (magnitude and phase) of the sequence components of the network line-to-line voltage for each simulated case. All the simulation results will be presented for $t \geq 0.2$ s. This procedure has been adopted to ensure that all DC capacitors of the MMC-STATCOM are charged and the SOGI and PLL circuits are operating in steady-state.

Table 5 – Network-side RMS line-to-line voltages for negative-sequence voltage compensation using the 3-phase 3-wire MMC-STATCOM

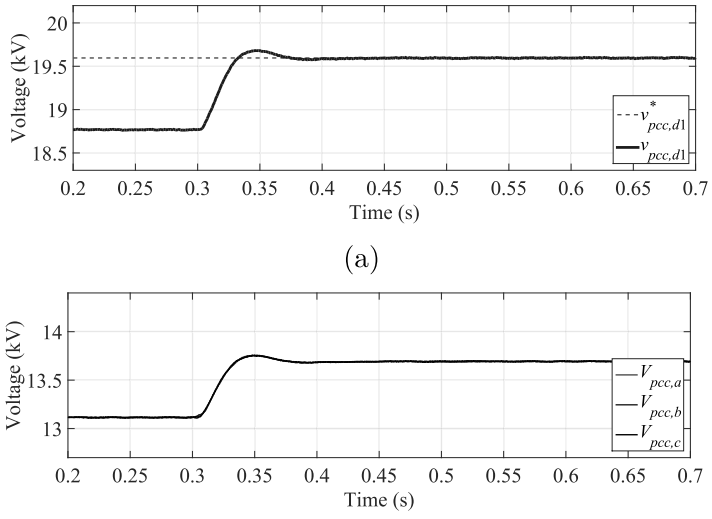
Case	**Voltage sequence component (kV)**		
	Positive	**Negative**	**Zero**
1	$22.92\angle 0°$	$0\angle 0°$	$0\angle 0°$
2	$24.00\angle 0°$	$0.6\angle -30°$	$0\angle 0°$
3	$22.92\angle 0°$	$0.6\angle -30°$	$0\angle 0°$

Source: Elaborated by the author (2021).

3.3.1 **Case 1**

In this first case, the network voltages are balanced, but their magnitude is less than the rated value (24 kV). Figures 43 (a) and (b) show the reference (dashed-line) and the direct-axis positive-sequence voltage at the PCC and the RMS values of the PCC voltages, respectively. Figures 44 (a) and (b) show the instantaneous three-phase voltages and currents at the MMC-STATCOM terminals, respectively. From $t = 0.2$ s to $t = 0.3$ s the MMC-STATCOM does not regulate the PCC voltages. It can be noted that the terminal voltages synthesized by the static compensator present a lower harmonic content due to the number of levels of the converter ($2n + 1 = 29$). In $t = 0.3$ s the MMC-STATCOM starts regulating the voltage at the PCC. The voltage controller forces the MMC-STATCOM to synthesize three-phase positive-sequence currents to restore the voltages at the PCC to its rated value. Figures 45 (a) and (b) show the upper and lower arm SM capacitor DC voltages of phase "a" and the upper arm SM capacitor DC voltages of the three-phases, respectively.

Figure 43 – Waveforms of the PCC voltages for the Case 1 in which the 3-phase 3-wire MMC-STATCOM regulates the positive-sequence voltage at the PCC.



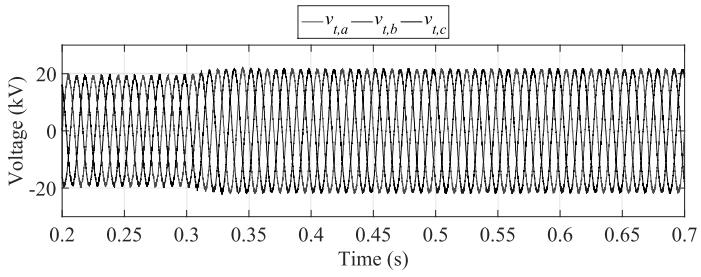
(a)

(b)

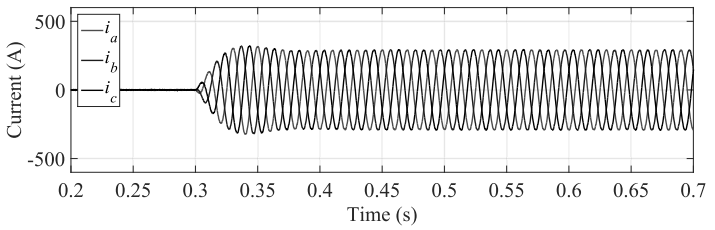
Caption: (a) reference signal and the direct-axis positive-sequence voltage at the PCC, (b) RMS values of the PCC voltages.

Source: Elaborated by the author (2021).

Figure 44 – Waveforms of the static compensator terminal voltages and currents for the Case 1 in which the 3-phase 3-wire MMC-STATCOM regulates the positive-sequence voltage at the PCC.



(a)

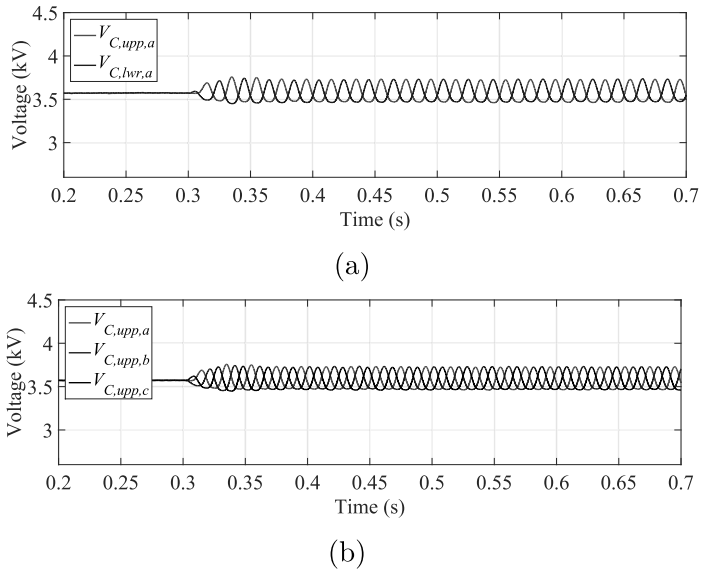


(b)

Caption: (a) voltages, (b) currents.

Source: Elaborated by the author (2021).

Figure 45 – Waveforms of the static compensator DC voltages for the Case 1 in which the 3-phase 3-wire MMC-STATCOM regulates the positive-sequence voltage at the PCC.



(a)

(b)

Caption: (a) upper and lower arm SM capacitor DC voltages of phase "a" and (b) upper arm SM capacitor DC voltages of the three phases.

Source: Elaborated by the author (2021).

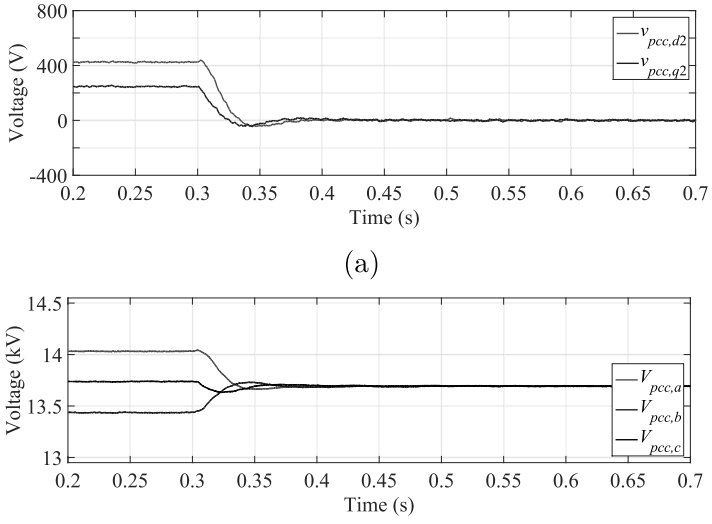
3.3.2 **Case 2**

In this second case the positive-sequence voltages are set to their nominal value, but the voltages at the PCC are unbalanced due to a presence of a negative-sequence component. Figures 46 (a) and (b) show the waveforms of the direct- and quadrature-axis negative-sequence voltages at the PCC and the RMS values of the PCC voltages, respectively. Figures 47 (a) and (b) show the instantaneous three-phase voltages and currents at the MMC-STATCOM terminals, respectively. From $t = 0.2$ s to $t = 0.3$ s the PCC voltages are unbalanced due to a presence of a negative-sequence voltage component. At $t = 0.3$ s the MMC-STATCOM starts compensating for negative-sequence unbalance. The control algorithm forces the MMC-STATCOM to synthesize negative-sequence currents at its terminals to compensate the negative-sequence voltages at the PCC. Figures 48 (a) and (b) show the upper and lower arm SM capacitor DC voltages of phase "a" and the upper arm SM capacitor DC voltages of the three-phases, respectively.

3.3.3 **Case 3**

In this last case the magnitude of the positive-sequence voltage is less than the rated value (24 kV) and the PCC voltage is unbalanced due to a presence of a negative-sequence voltage component. Figures 49 (a), (b) and (c) show the RMS values of the phase-voltages

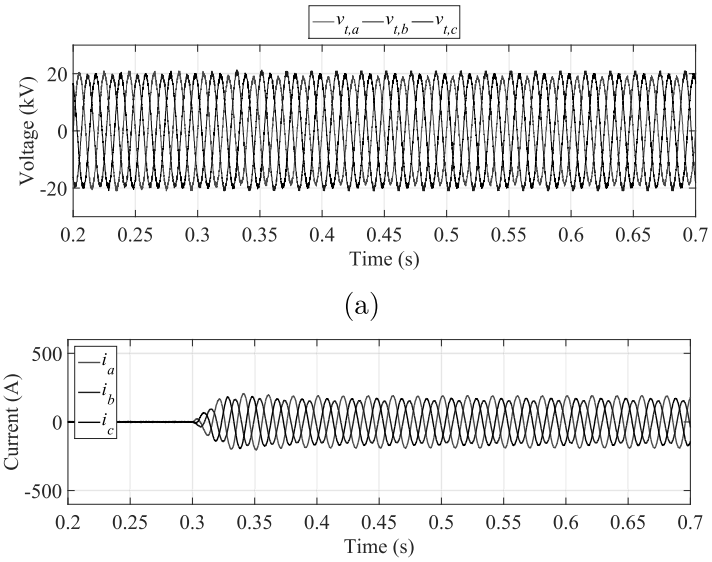
Figure 46 – Waveforms of the PCC voltages for the Case 2 in which the 3-phase 3-wire MMC-STATCOM compensates the negative-sequence voltage at the PCC.



Caption: (a) direct- and quadrature-axis negative-sequence voltages at the PCC, (b) RMS values of the PCC voltages.

Source: Elaborated by the author (2021).

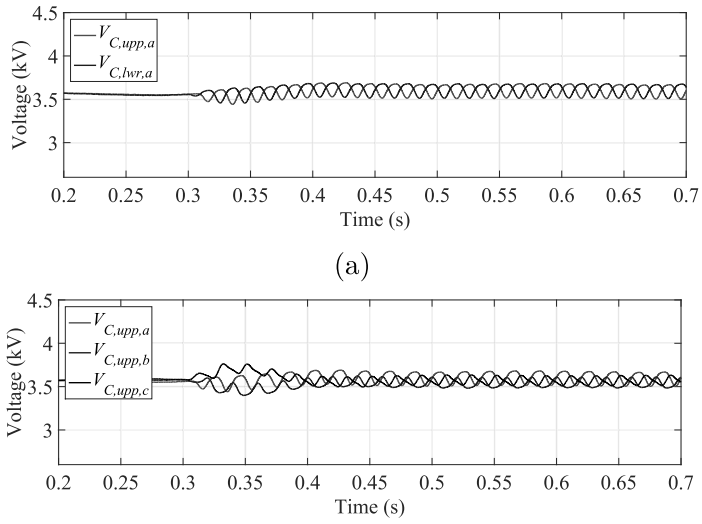
Figure 47 – Waveforms of the static compensator terminal voltages and currents for the Case 2 in which the 3-phase 3-wire MMC-STATCOM compensates the negative-sequence voltage at the PCC.



Caption: (a) voltages, (b) currents.

Source: Elaborated by the author (2021).

Figure 48 – Waveforms of the static compensator DC voltages for the Case 2 in which the 3-phase 3-wire MMC-STATCOM compensates the negative-sequence voltage at the PCC.



(a)

(b)

Caption: (a) upper and lower arm SM capacitor DC voltages of phase "a" and (b) upper arm SM capacitor DC voltages of the three phases.

Source: Elaborated by the author (2021).

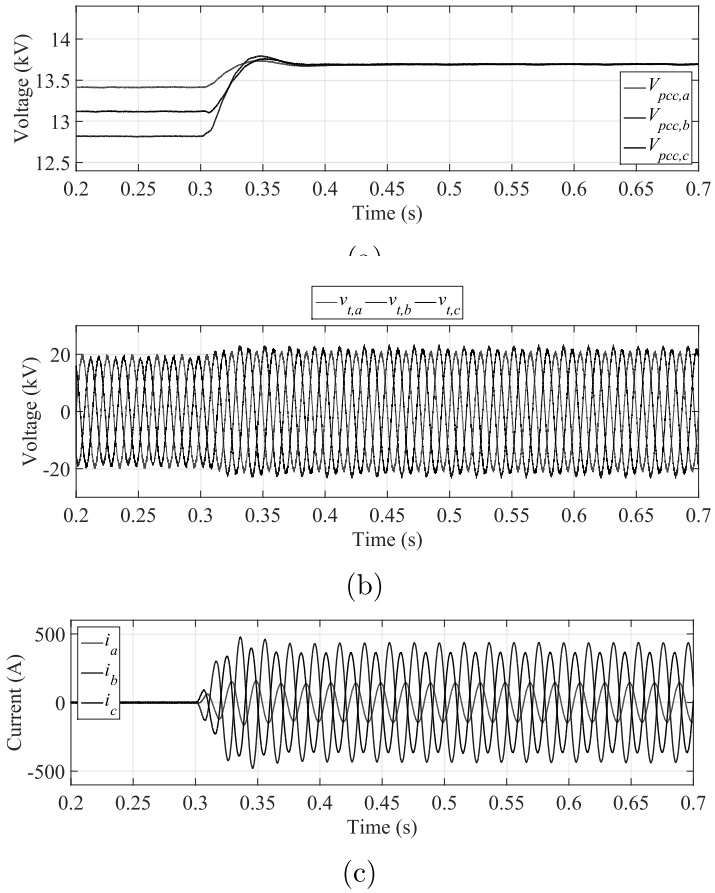
at the PCC and the waveforms of the MMC-STATCOM terminal voltages and currents, respectively. From $t = 0.2$ s to $t = 0.3$ s the positive-sequence voltages at the PCC are below the system nominal value and they are also unbalanced due to a negative-sequence voltage component. At $t = 0.3$ s the MMC-STATCOM starts synthesizing currents at its terminals in order to regulate the PCC voltage at the system nominal value (24 kV) and to compensate the negative-sequence voltage unbalance.

Figures 50 (a), (b) and (c) show the SM voltages of the upper and lower arms of the phases "a", "b" and "c" of the MMC-STATCOM, respectively. It can be noted that the DC voltages are regulated simultaneously with the two other strategies of voltage compensation.

3.4 CONCLUSIONS

This chapter presented a negative-sequence voltage compensation strategy of a distribution network by using a three-phase three-wire static synchronous compensator based on the modular multilevel converter. Mathematical models, in the synchronous reference frame, were developed to design positive-sequence voltage and current control loops in order to allow the converter to regulate the positive-sequence voltage at the point of common coupling. Based on the methodology presented for the positive-sequence, the negative-sequence current and voltage control loops were developed and designed so that

Figure 49 – Waveforms of the PCC voltages and static compensator terminal voltages and currents for the Case 3 in which the 3-phase 3-wire MMC-STATCOM regulates the positive- and negative-sequence voltages at the PCC.



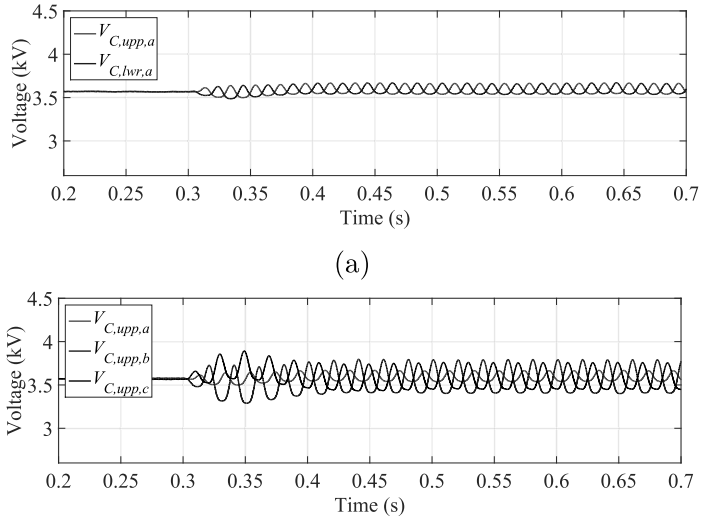
Caption: (a) RMS values of the PCC voltages, (b) MMC-STATCOM terminal voltages and (c) MMC-STATCOM terminal currents.

Source: Elaborated by the author (2021).

the static compensator could compensate the negative-sequence voltages at the point of connection of an unbalanced distribution network. A low-pass filter was connected to the feedback of the DC voltage control loop in order to filter the signal measured at the DC terminals of the converter. Results of digital simulations were used to validate the proposed control strategies and the designs of the static compensator's controllers. It was presented that the MMC-STATCOM can synthesize positive- and negative-sequence currents with low harmonic content to balance the voltages at the point of common coupling. Moreover, the SM DC voltages of the static compensator were regulated simultaneously with the positive- and negative-sequence voltage compensation strategies. Further results, including experimental results obtained with a small-scale prototype, are shown in (DUARTE *et al.*, 2021) where this chapter is based.

In the next chapter it will be presented a control strategy for a three-phase four-wire

Figure 50 – Waveforms of the static compensator DC voltages for the Case 3 in which the 3-phase 3-wire MMC-STATCOM regulates the positive- and negative-sequence voltages at the PCC.



(a)

(b)

Caption: (a) upper and lower arm SM capacitor DC voltages of phase "a" and (b) upper arm SM capacitor DC voltages of the three phases.

Source: Elaborated by the author (2021).

MMC-STATCOM. This strategy will allow the converter to compensate for zero-sequence voltage imbalance at the point of common coupling.

4 ZERO-SEQUENCE VOLTAGE COMPENSATION OF A DISTRIBUTION NETWORK THROUGH A THREE-PHASE FOUR-WIRE MMC-STATCOM

This chapter presents the methodology published in Duarte *et al.* (2019) to control a four-wire three-phase MMC-STATCOM in order to compensate the zero-sequence voltage at the PCC of a four-wire three-phase medium-voltage distribution network (SALLAM; MALIK, 2018). The mathematical models used to derive the zero-sequence current and voltage control loops for the MMC-STATCOM will be shown. Digital simulations will be used to demonstrate the effectiveness of the proposed compensation strategy.

4.1 INTRODUCTION

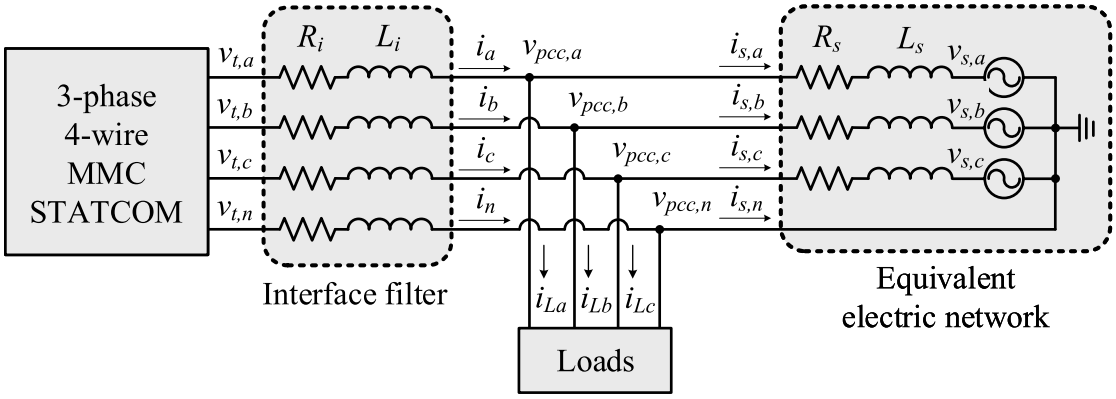
In the previous chapter, the three-phase three-wire MMC-STATCOM was connected to a medium-voltage distribution network to regulate the positive-sequence voltage and to compensate for negative-sequence voltage imbalance at the PCC. However, it cannot compensate for zero-sequence voltage imbalances. Moreover, the papers aforementioned in Section 3.1 do not present mathematical models for the zero-sequence voltage control at the PCC. The lack of these models makes difficult the use of a mathematical methodology to design the gains of the AC voltage controllers.

Thus, the main objective of this chapter is to present a zero-sequence voltage compensation strategy in distribution networks by using the three-phase four-wire MMC-STATCOM. Mathematical modellings, in the synchronous reference frame, are presented and used to derive the zero-sequence control loops and to design the controller gains of the static compensator. The MMC-STATCOM will be controlled to synthesize currents at its terminals in order to regulate the positive-sequence voltage at the nominal value and to compensate the zero-sequence voltage at the PCC. Results of digital simulations of the four-wire three-phase MMC-STATCOM connected to a medium-voltage distribution network with unbalanced voltages will be used to demonstrate the effectiveness of the voltage compensation strategy.

4.2 MATHEMATICAL MODELLING AND CONTROL OF THE THREE-PHASE FOUR-WIRE MMC-STATCOM

Diagram 25 depicts the three-phase four-wire MMC-STATCOM connected to an equivalent distribution network through four first-order low-pass passive filters (L_i, R_i). The electric network was modelled by an ideal three-phase source series-connected with an impedance $(R_s + \jmath\omega_s L_s)$, where $\omega_s = 2\pi f_s$ is the fundamental angular frequency of the electric system. The topology of the three-phase four-wire MMC-STATCOM is the same of that shown in Diagram 11.

Diagram 25 – 3-phase 4-wire MMC-STATCOM connected to an equivalent electric network and loads.



Source: Elaborated by the author (2021).

Neglecting the harmonics generated by the MMC-STATCOM and considering that the phase-to-neutral voltages at the PCC ($v_{pcc,an}$, $v_{pcc,bn}$, $v_{pcc,cn}$) are unbalanced, the following dynamic equations can be written, in the $\alpha\beta 0$ coordinates, for the currents synthesized by the MMC-STATCOM of Diagram 25:

$$L_{eq}\frac{di_\alpha}{dt} = -R_{eq}i_\alpha + v_{t,\alpha} - v_{pcc,\alpha} \tag{4.1}$$

$$L_{eq}\frac{di_\beta}{dt} = -R_{eq}i_\beta + v_{t,\beta} - v_{pcc,\beta} \tag{4.2}$$

$$L_{eq}\frac{di_0}{dt} = -R_{eq}i_0 + v_{t,0} - v_{pcc,0} \tag{4.3}$$

where i_α, i_β and i_0 are the instantaneous currents at the MMC-STATCOM terminals; $v_{pcc,\alpha}$, $v_{pcc,\beta}$ and $v_{pcc,0}$ are the instantaneous voltages at the PCC; $v_{t,\alpha}$, $v_{t,\beta}$ and $v_{t,0}$ are the instantaneous voltages at the MMC-STATCOM terminals; $L_{eq} = (L_i + L_f/2)$ and $R_{eq} = (R_i + R_f/2)$ are the equivalent inductance and resistance, respectively; the $\alpha\beta 0$ transformation ensures amplitude invariance as shown in (3.1).

The model presented above has the advantage of isolating the positive- and negative-sequence quantities, which are in (4.1) and (4.2), from the zero-sequence variables, which lies in (4.3). This approach will allow controlling the fourth-leg of the MMC-STATCOM as a single-phase converter to compensate for the zero-sequence unbalance at the PCC. Thus, for the sake of simplicity, in the following sections the unbalanced network will be considered only with the presence of positive- and zero-sequence components.

Despite the advantages of representing the voltages and currents in the $\alpha\beta 0$ coordinates, the use of the synchronous reference frame makes the design of the MMC-STATCOM controllers easier. Thus, applying the $\alpha\beta \rightarrow dq$ transformation (Appendix D) in (4.1) and

(4.2) yields:

$$L_{eq}\frac{di_{d1}}{dt} = +\omega L_{eq} i_{q1} - R_{eq} i_{d1} + v_{t,d1} - v_{pcc,d1} \tag{4.4}$$

and

$$L_{eq}\frac{di_{q1}}{dt} = -\omega L_{eq} i_{d1} - R_{eq} i_{q1} + v_{t,q1} - v_{pcc,q1}, \tag{4.5}$$

where i_{d1} and i_{q1} are the direct- and quadrature-axis instantaneous currents synthesized by the MMC-STATCOM; $v_{t,d1} = m_{d1}(V_{dc}/2)$ and $v_{t,q1} = m_{q1}(V_{dc}/2)$ are the direct- and quadrature-axis voltages at the MMC-STATCOM terminals; m_{d1} and m_{q1} are the modulation indexes for a PWM sinusoidal strategy; V_{dc} is the MMC-STATCOM DC terminal voltage; $v_{pcc,d1}$ and $v_{pcc,q1}$ are the direct- and quadrature-axis voltages at the PCC; ω is the fundamental angular frequency of the PCC voltages and the subscript $(_1)$ denotes the positive-sequence.

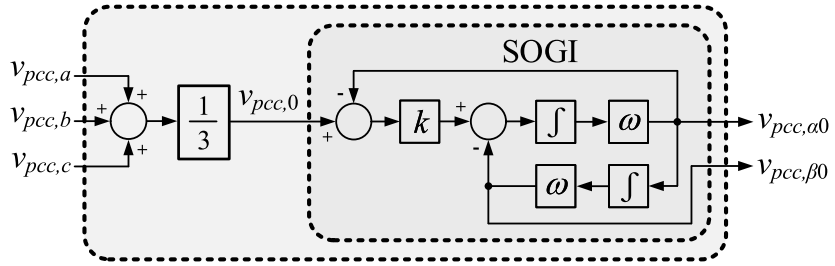
The mathematical modelling given by (4.4) and (4.5) for the MMC-STATCOM's positive-sequence currents is the same given by (3.5) and (3.6) presented in the Subection 3.2.2. This modelling allowed to design the positive-sequence current controller for the MMC-STATCOM. Thus, in this chapter it will be presented only the mathematical modellings to design the zero-sequence voltage and current control loops for the three-phase four-wire MMC-STATCOM.

4.2.1 **The zero-sequence current control**

As previously mentioned, the fourth-leg of the MMC-STATCOM can be controlled as a single-phase converter. However, since it is not possible directly to use the synchronous reference frame transformation in the zero-sequence variables, the zero-sequence current control strategy requires some modifications in the algorithm presented in Subection 3.2.1. To overcome this constraint, a SOGI (RODRIGUEZ *et al.*, 2006) and a transport delay buffer (FURTADO *et al.*, 2014) will be used to generate 90-degrees shift-delay signals for the zero-sequence voltage and current, respectively.

Diagram 26 shows the block diagram for the algorithm used to convert the zero-sequence voltage at the PCC into a fictitious $\alpha\beta$ reference frame. The output signal $v_{pcc,\alpha 0}$ tracks the instantaneous zero-sequence voltage $v_{pcc,0}$ while the voltage $v_{pcc,\beta 0}$ is lagged from $v_{pcc,\alpha 0}$. The SOGI has the advantage of blocking input voltage harmonics. This feature may be interesting if there are triplen harmonics (*e.g.* 3^{rd}, 9^{th}, etc.), which have zero-sequence characteristic, at the input voltage. It also has the ability to be frequency adaptive. This quality could be used to minimize the estimation error of the zero-sequence quadrature voltages. The SOGI also does not require buffers to store the measured voltages, diminishing memory usage in the case of digital implementation.

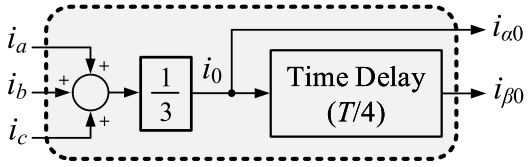
Diagram 26 – Block diagram for the SOGI circuit used to generate the zero-sequence quadrature voltages.



Source: Reproduced from (DUARTE *et al.*, 2019).

Despite the good performance of the SOGI, the currents synthesized by the MMC-STATCOM present a faster dynamic behaviour than the voltage measured at the PCC. Thus, in order not to compromise the ability of the zero-sequence current control loop to track the reference signal, a transport delay buffer is used to generate the fictitious component $i_{\beta 0}$ for the zero-sequence current $i_0 = i_{\alpha 0}$ (FURTADO *et al.*, 2014). Diagram 27 shows the block diagram for the transport delay buffer, where $T = (1/f)$ is the fundamental period of the zero-sequence current.

Diagram 27 – Block diagram for the transport delay buffer used to generate the zero-sequence quadrature currents.



Source: Reproduced from (DUARTE *et al.*, 2019).

Then, using the circuits of Diagram 26 and Diagram 27 to transform the zero-sequence voltage and current given in (4.3) into two quadrature fictitious variables in the $\alpha\beta$-coordinates, the following system of equations can be written:

$$L_{eq}\frac{di_{\alpha 0}}{dt} = -R_{eq}i_{\alpha 0} + v_{t,\alpha 0} - v_{pcc,\alpha 0} \tag{4.6}$$

and

$$L_{eq}\frac{di_{\beta 0}}{dt} = -R_{eq}i_{\beta 0} + v_{t,\beta 0} - v_{pcc,\beta 0}, \tag{4.7}$$

where $v_{t,\alpha 0}$ and $v_{t,\beta 0}$ are the MMC-STATCOM instantaneous zero-sequence terminal voltages.

Applying the transformation given in Appendix D in (4.6) and (4.7), the dynamics of the zero-sequence current in a fictitious synchronous reference frame is given by:

$$L_{eq}\frac{di_{d0}}{dt} = +\omega L_{eq} i_{q0} - R_{eq} i_{d0} + v_{t,d0} - v_{pcc,d0} \tag{4.8}$$

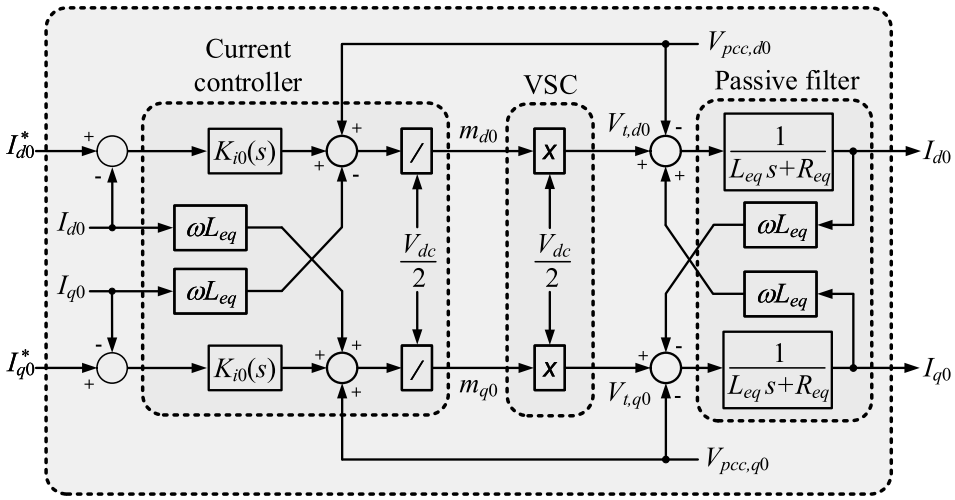
and

$$L_{eq}\frac{di_{q0}}{dt} = -\omega L_{eq} i_{d0} - R_{eq} i_{q0} + v_{t,q0} - v_{pcc,q0}, \tag{4.9}$$

where i_{d0} and i_{q0} are the MMC-STATCOM currents; $v_{pcc,d0}$ and $v_{pcc,q0}$ are the voltages at the PCC; $v_{t,d0} = m_{d0}(V_{dc}/2)$ and $v_{t,q0} = m_{q0}(V_{dc}/2)$ are the MMC-STATCOM terminal voltages; m_{d0} and m_{q0} are the MMC-STATCOM modulation indexes and ω is the fundamental angular frequency of the positive-sequence voltage at the PCC. The subscript $(_0)$ is used in the above equations to denote the zero-sequence quantities.

Based on (4.8) and (4.9), and following the same steps used in Subection 3.2.2 to design the positive-sequence current control loops, it is possible to draw the block diagram of Diagram 28 to regulate the currents I_{d0} and I_{q0}. In this figure, the design of loops to compensate the cross-coupling between the zero-sequence currents and the effect of the direct- and quadrature-axis PCC voltages makes it possible to redraw this block diagram as shown in Diagram 29. In this way, the gains for the zero-sequence current controller $K_{i0}(s) = (k_{p,i0} + k_{i,i0}/s)$ can be chosen equal to $k_{p,i0} = (L_{eq}/\tau_{i0})$ and $k_{i,i0} = (R_{eq}/\tau_{i0})$, where τ_{i0} is the desired zero-sequence time constant.

Diagram 28 – Block diagram for the direct- and quadrature-axis zero-sequence current control loops.

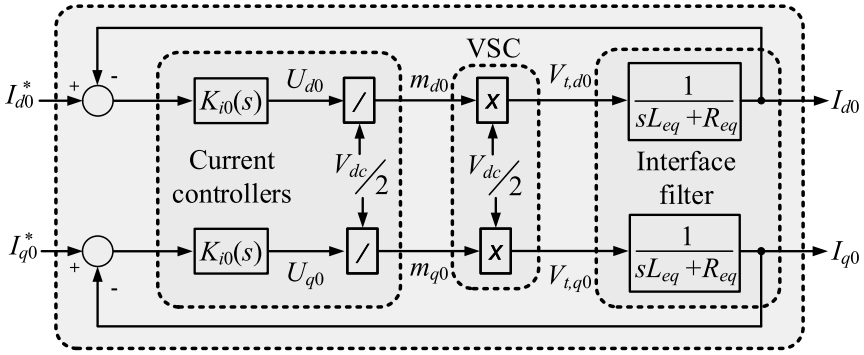


Source: Reproduced from (DUARTE *et al.*, 2019).

Then, the zero-sequence modulation index m_0 is calculated by:

$$m_0 = \cos(\rho) m_{d0} - \sin(\rho) m_{q0}, \tag{4.10}$$

Diagram 29 – Simplified block diagram for the direct- and quadrature-axis zero-sequence current control loops.



Source: Reproduced from (DUARTE *et al.*, 2019).

where $\rho = (\omega t + \phi)$ is the angle of the positive-sequence voltage at the PCC, where ω and ϕ are the angular frequency and the phase of ρ, respectively.

By using (4.10), it is possible to calculate the modulation index m_n for the fourth-leg of the MMC-STATCOM as follows:

$$m_n = -(m'_a + m'_b + m'_c), \tag{4.11}$$

where $m'_k = (m_k + m_0)$ and $k \in \{a, b, c\}$ are the phases of the MMC-STATCOM.

4.2.2 The zero-sequence voltage compensation

Again, starting from the network-side terminals of Diagram 25, however using here the SOGI circuit (Diagram 26) and the transport delay buffer (Diagram 27), the following relations can be written in the dq-frame for the zero-sequence voltage at the PCC:

$$v_{pcc,d0} = L_{s0}\frac{di_{s,d0}}{dt} - \omega L_{s0} i_{s,q0} + R_{s0} i_{s,d0} + v_{s,d0} \tag{4.12}$$

and

$$v_{pcc,q0} = L_{s0}\frac{di_{s,q0}}{dt} + \omega L_{s0} i_{s,d0} + R_{s0} i_{s,q0} + v_{s,q0}, \tag{4.13}$$

where R_{s0} and L_{s0} are the zero-sequence equivalent resistance and inductance of the network, respectively; $v_{pcc,d0}$ and $v_{pcc,q0}$ are the zero-sequence voltages at the PCC; $v_{s,d0} = \hat{V}_{s0}\cos(\omega_s t + \phi_{s0} - \rho)$ and $v_{s,q0} = \hat{V}_{s0}\sin(\omega_s t + \phi_{s0} - \rho)$; $\hat{V}_{s0}$ and ϕ_{s0} are the peak value and the phase of the zero-sequence network voltages, respectively; $\rho = (\omega t + \phi)$ is the angle tracked by the PLL, where ω and ϕ are the fundamental angular frequency and phase angle of the positive-sequence voltage at the PCC, respectively.

The comparison of (4.12) and (4.13) with (3.13) and (3.14) allows to use the same steps presented in the Subection 3.2.3 to obtain small-signal transfer functions for the zero-sequence voltages at the PCC, resulting in:

$$\tilde{V}_{pcc,d0}(s) = \ G_{d0}(s)\tilde{I}_{d0}(s) - G_{q0}(s)\tilde{I}_{q0}(s) - G_{d0}(s)\tilde{I}_{L,d0}(s) + G_{q0}(s)\tilde{I}_{L,q0}(s) \quad (4.14)$$

and

$$\tilde{V}_{pcc,q0}(s) = \ G_{d0}(s)\tilde{I}_{q0}(s) + G_{q0}(s)\tilde{I}_{d0}(s) - G_{d0}(s)\tilde{I}_{L,q0}(s) - G_{q0}(s)\tilde{I}_{L,d0}(s), \quad (4.15)$$

where $G_{d0}(s) = (R_{s0} + sL_{s0})$; $G_{q0}(s) = \bar{\omega}L_{s0}$; $\tilde{I}_{d0}(s)$ and $\tilde{I}_{q0}(s)$ are the direct- and quadrature-axis currents synthesized by the MMC-STATCOM, respectively; $\tilde{I}_{L,d0}(s)$ and $\tilde{I}_{L,q0}(s)$ are the direct- and quadrature-axis currents drained by the load, respectively.

The analysis of (4.14) and (4.15) shows that, although the voltages $\tilde{V}_{pcc,d0}(s)$ and $\tilde{V}_{pcc,q0}(s)$ depend on the currents drained by the load, they can be controlled by the currents $\tilde{I}_{d0}(s)$ and $\tilde{I}_{q0}(s)$, synthesized by the MMC-STATCOM.

Diagram 30 shows the zero-sequence voltage control block diagram. Unlike the positive-sequence voltage control, two controllers will be used here, one for the direct-axis and another for the quadrature-axis. The block $K_{v0}(s)$ represents the zero-sequence voltage controller while $H_{i0}(s)$ represents the closed-loop transfer function of the zero-sequence current control loop.

If the zero-sequence current controller is designed in such a way that the time constant of the closed-loop transfer function of the current controller is much smaller than the voltage controller one, the transfer function $H_{i0}(s)$ can be replaced by an unitary gain and, the closed-loop transfer function of the zero-sequence voltage control loop is given by:

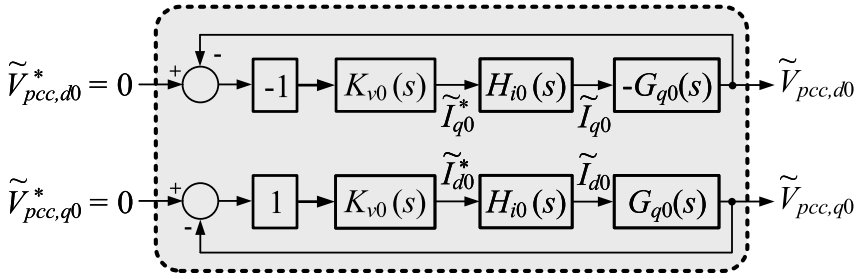
$$H_{v0}(s) = \frac{1}{s\tau_{v0} + 1}, \quad (4.16)$$

where $\tau_{v0} = 1/(k_{v0}\bar{\omega}L_{s0})$ is the time constant of the zero-sequence voltage control loop and k_{v0} is the gain of the integral controller $K_{v0}(s) = k_{v0}/s$. The gain k_{v0} can be calculated by choosing the desired time-constant for $H_{v0}(s)$.

4.3 DIGITAL SIMULATION OF THE ZERO-SEQUENCE VOLTAGE COMPENSATION STRATEGY

Diagram 31 shows the static compensator connected to a distribution network. The circuit of Diagram 31 and the three-phase four-wire MMC-STATCOM, similar to that shown in Diagram 11, with all its controllers were modelled in an electromagnetic transient program in order to demonstrate the compensation of the PCC voltages. The

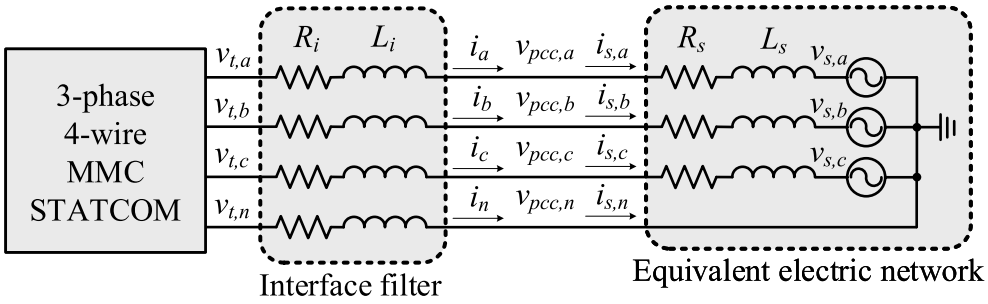
Diagram 30 – Block diagram for the direct- and quadrature-axis zero-sequence voltage control loops.



Source: Reproduced from (DUARTE *et al.*, 2019).

parameters of the electric network, MMC-STATCOM, digital filters and controllers are given in Tables 8, 9, 10 and 6, respectively. Each leg of the MMC-STATCOM was modelled with 28 SMs connected in series, 14 SMs in the upper arm and 14 SMs in the lower arm.

Diagram 31 – 3-phase 4-wire MMC-STATCOM connected to an equivalent electric network.



Source: Elaborated by the author (2021).

Table 6 – Controller gains of the 3-phase 4-wire MMC-STATCOM with 14 SMs per arm.

Controller	**Gain**	**Value**
$K_{i1}(s)$	$k_{p,i1}$	$31.6\ \mathrm{V\,A^{-1}}$
	$k_{i,i1}$	$0.5\ \mathrm{kV\,A^{-1}\,s^{-1}}$
$K_{v1}(s)$	k_{v1}	$40.3\ \mathrm{A\,V^{-1}\,s^{-1}}$
$K_{i2}(s)$	$k_{p,i2}$	$31.6\ \mathrm{V\,A^{-1}}$
	$k_{i,i2}$	$0.5\ \mathrm{kV\,A^{-1}\,s^{-1}}$
$K_{v2}(s)$	k_{v2}	$40.3\ \mathrm{A\,V^{-1}\,s^{-1}}$
$K_{i0}(s)$	$k_{p,i0}$	$31.6\ \mathrm{V\,A^{-1}}$
	$k_{i,i0}$	$0.5\ \mathrm{kV\,A^{-1}\,s^{-1}}$
$K_{v0}(s)$	k_{v0}	$40.3\ \mathrm{A\,V^{-1}\,s^{-1}}$
$K_{vdc}(s)$	$k_{p,vdc}$	$12.2\ \mathrm{\mu A\,V^{-2}}$
	$k_{i,vdc}$	$1.22\ \mathrm{\mu A\,V^{-2}\,s^{-1}}$
$K_{cir}(s)$	$k_{p,cir}$	$6.07\ \mathrm{V\,A^{-1}}$
	$k_{i,cir}$	$632\ \mathrm{V\,A^{-1}\,s^{-1}}$

Source: Elaborated by the author (2021).

All the MMC-STATCOM controllers were implemented digitally. They were discretized using the bilinear approximation, considering a sampling frequency equal to 25 kHz. Since the sampling frequency is ten times greater than the bandwidth of the controllers the distortion of the output signals caused by the discretization of the controllers will be less than 3% (BUSO; MATTAVELLI, 2015).

A PD-PWM technique is used to generate the switching pattern for the IGBTs of the compensator. The voltages of the upper and lower arm SMs are regulated using an algorithm that measures and sorts the SMs in descending order according to their DC voltages, as proposed in (GHETTI *et al.*, 2017), while the DC terminal voltage of the MMC-STATCOM is regulated by using the DC voltage control loop of Diagram 22.

Three cases will be investigated: (*i*) positive-sequence voltage regulation, (*ii*) zero-sequence voltage compensation and (*iii*) both strategies working simultaneously. In all cases, the circulating current control is active. The imbalance in the PCC voltages was simulated by connecting three voltage sources in series, for the positive-, negative- and zero-sequence components, with each phase of the ending-side of the network. Table 7 shows the RMS values (magnitude and phase) of the network line-to-line voltage sequence components for each simulated case. All the simulation results will be presented for $t \geq 0.2$ s. This procedure has been adopted to ensure that all DC capacitors of the MMC-STATCOM are charged and the SOGI and PLL circuits are operating in steady-state.

Table 7 – Network-side RMS line-to-line voltages for zero-sequence voltage compensation using the 3-phase 4-wire MMC-STATCOM

Case	**Voltage sequence component (kV)**		
	Positive	**Negative**	**Zero**
1	$22.92\angle 0°$	$0\angle 0°$	$0\angle 0°$
2	$24.00\angle 0°$	$0\angle 0°$	$0.6\angle -30°$
3	$22.92\angle 0°$	$0\angle 0°$	$0.6\angle -30°$

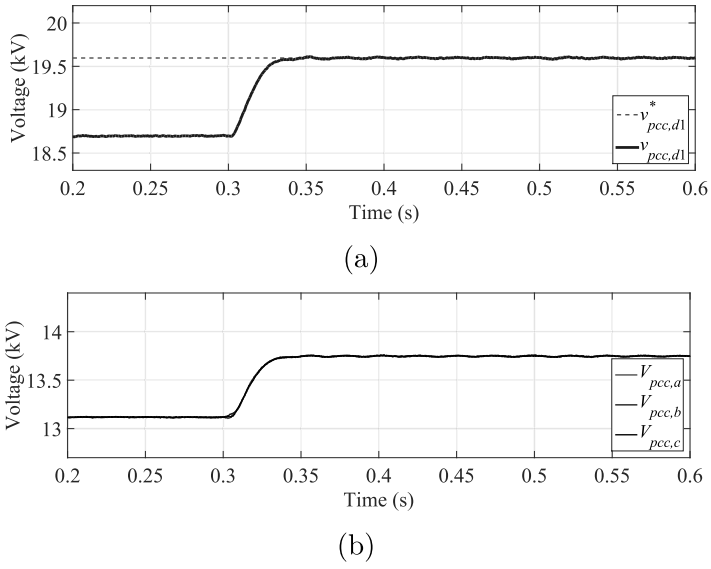
Source: Elaborated by the author (2021).

4.3.1 **Case 1**

In this first case, the network voltages are balanced, but their magnitude is less than the rated value (24 kV). Figures 51 (a) and (b) show the reference (dashed-line) and the direct-axis positive-sequence voltage at the PCC and the RMS values of the PCC voltages. Figures 52 (a) and (b) show the instantaneous three-phase voltages and currents at the MMC-STATCOM terminals, respectively. From $t = 0.2$ s to $t = 0.3$ s the MMC-STATCOM does not regulate the PCC voltages. It can be noted that the terminal voltages of the MMC-STATCOM present low harmonic content due to the number of levels of the synthesized voltages ($2n + 1 = 29$). At $t = 0.3$ s the static compensator starts regulating the voltage at the PCC. The voltage controller forces the MMC-STATCOM to

synthesize three-phase positive-sequence currents to restore the voltages at the PCC to its rated value.

Figure 51 – Waveforms of the PCC voltages for the Case 1 in which the 3-phase 4-wire MMC-STATCOM regulates the positive-sequence voltage at the PCC.



Caption: (a) reference signal and the direct-axis positive-sequence voltage at the PCC and (b) RMS values of the PCC voltages.

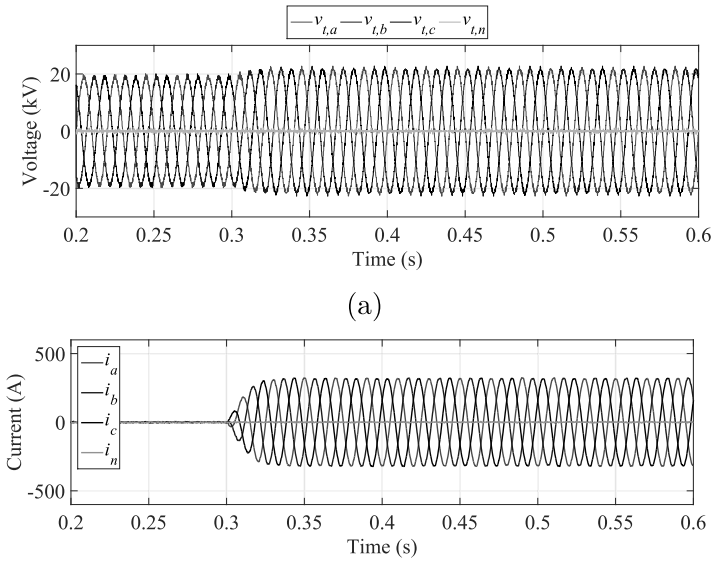
Source: Elaborated by the author (2021).

Figures 53 (a) and (b) show the SM voltages of the upper and lower arms of the phase "a" and the fourth-leg of the MMC-STATCOM, respectively. It can be noted in Figure 53 (b) that the DC voltages of the arms connected to the neutral do not oscillate since $i_n = 0$.

4.3.2 **Variation of the grid impedance**

The performance of the PCC voltage control loops of the MMC-STATCOM will depend on the value of the network equivalent inductance, as shown in (3.22). Figures 54 (a) and (b) show the phase "a" waveforms of the MMC-STATCOM terminal current and the direct-axis positive-sequence voltage at the PCC for the Case 1 in which the MMC-STATCOM compensates the positive-sequence voltage at the PCC, considering a variation of ± 20% of the grid impedance value ($0.8L_s$, L_s and $1.2L_s$), respectively. The waveforms of Figure 54 (b) demonstrate that the PCC voltage tracks the reference signal in steady-state even when the equivalent impedance varies. If the inductance value is low, a high current level will be required to perform the voltage regulation. On the other hand, if the inductance value is high, a low current level will be used to perform the same task. In all cases, the compensation will be limited by the capacity of the MMC-STATCOM.

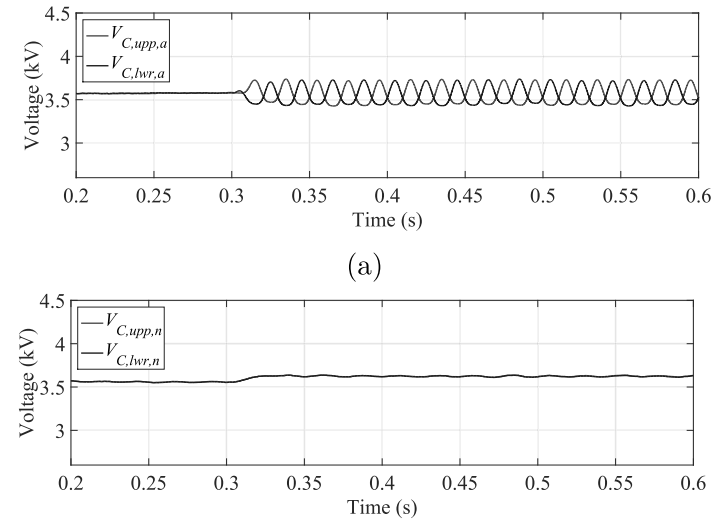
Figure 52 – Waveforms of the static compensator terminal voltages and currents for the Case 1 in which the 3-phase 4-wire MMC-STATCOM regulates the positive-sequence voltage at the PCC.



Caption: (a) voltages and (b) currents.

Source: Elaborated by the author (2021).

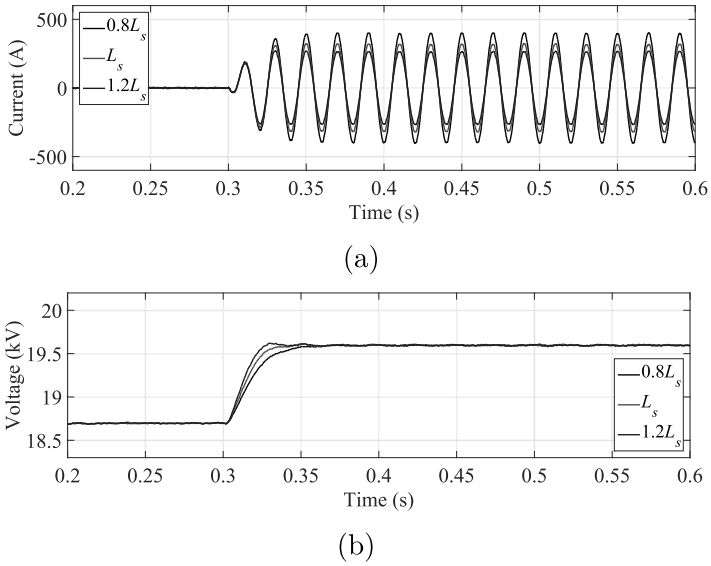
Figure 53 – Waveforms of the static compensator DC voltages for the Case 1 in which the 3-phase 4-wire MMC-STATCOM regulates the positive-sequence voltage at the PCC.



Caption: (a) upper and lower arm SM capacitor DC voltages of phase "a" and (b) upper and lower arm SM capacitor DC voltages of neutral.

Source: Elaborated by the author (2021).

Figure 54 – Performance of the proposed strategy when the impedance of the electric network vary.



Caption: (a) phase "a" terminal current of the MMC-STATCOM and (b) direct-axis positive-sequence voltage at the PCC.

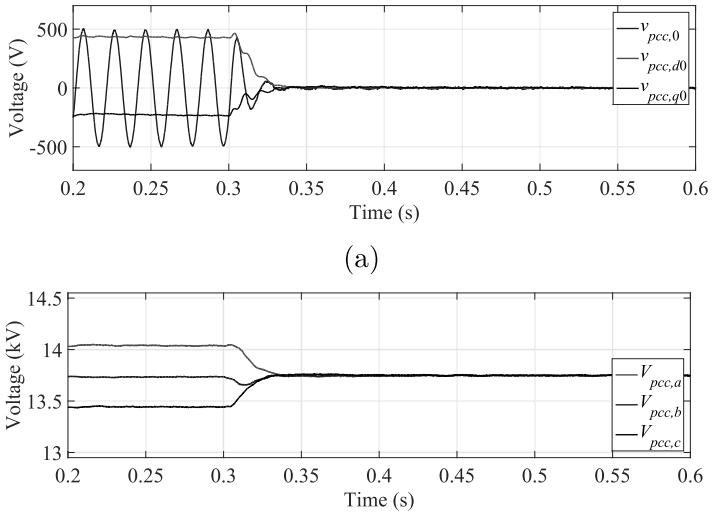
Source: Elaborated by the author (2021).

4.3.3 **Case 2**

In this second case the positive-sequence voltages are set to their nominal value, but the voltages at the PCC are unbalanced due to a presence of a zero-sequence component. Figures 55 (a) and (b) show the waveforms of the zero-sequence voltage at the PCC and its direct- and quadrature-axis components and the RMS values of the PCC voltages, respectively. Figures 56 (a) and (b) show the instantaneous three-phase voltages and currents at the MMC-STATCOM terminals, respectively. From $t = 0.2$ s to $t = 0.3$ s the PCC voltages are unbalanced due to a presence of a zero-sequence voltage component. At $t = 0.3$ s the MMC-STATCOM starts compensating for zero-sequence voltage imbalance. The control algorithm forces the MMC-STATCOM to synthesize zero-sequence currents at its terminals to compensate the zero-sequence voltages at the PCC. It is important to mention that the fourth-leg of the MMC-STATCOM should be designed to synthesize a neutral current three times greater than the phase currents, as shown in Figure 56 (b).

Figures 57 (a) and (b) show the SMs voltages of the upper and lower arms of the phase "a" and of the fourth-leg of the MMC-STATCOM, respectively. It can be noted in Figure 57 (b) that the DC voltages of the arm connected to the neutral start oscillating at $t = 0.3$ s due to the neutral current synthesized by the MMC-STATCOM.

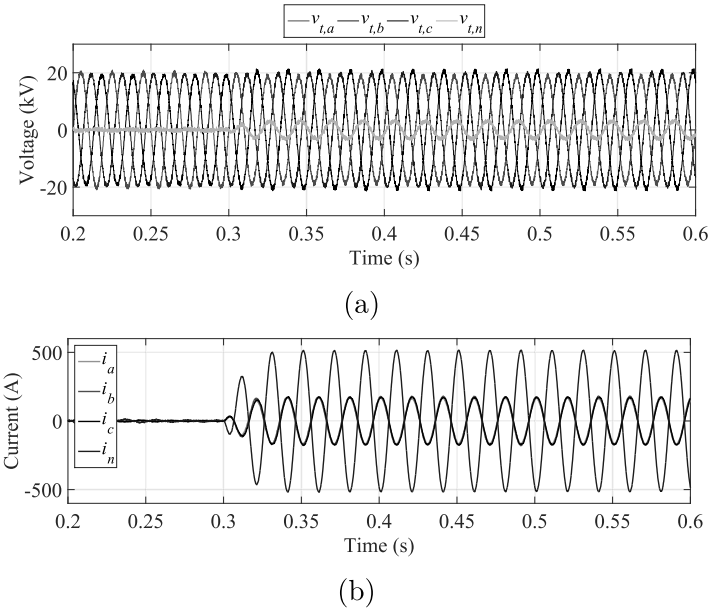
Figure 55 – Waveforms of the PCC voltages for the Case 2 in which the 3-phase 4-wire MMC-STATCOM compensates the zero-sequence voltage at the PCC.



Caption: (a) zero-sequence voltage at the PCC and (b) RMS values of the PCC voltages.

Source: Elaborated by the author (2021).

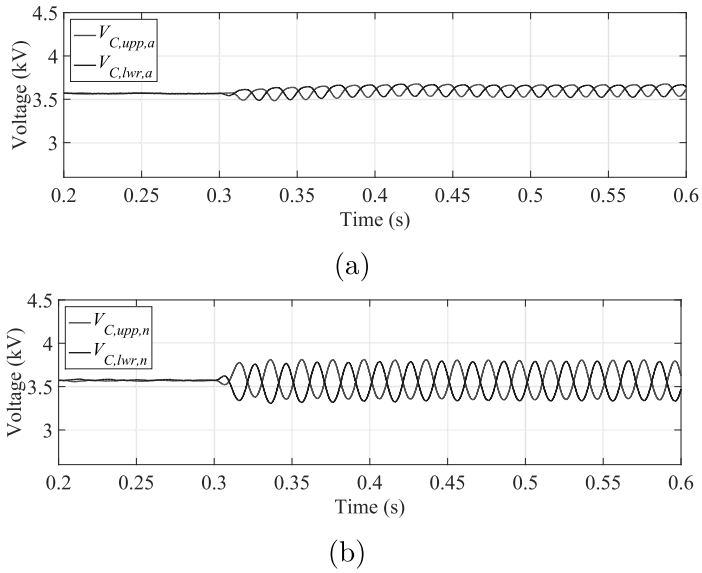
Figure 56 – Waveforms of the static compensator terminal voltages and currents for the Case 2 in which the 3-phase 4-wire MMC-STATCOM compensates the zero-sequence voltage at the PCC.



Caption: (a) voltages and (b) currents.

Source: Elaborated by the author (2021).

Figure 57 – Waveforms of the static compensator DC voltages for the Case 2 in which the 3-phase 4-wire MMC-STATCOM compensates the zero-sequence voltage at the PCC.



Caption: (a) upper and lower arm SM capacitor DC voltages of phase "a" and (b) upper and lower arm SM capacitor DC voltages of neutral.

Source: Elaborated by the author (2021).

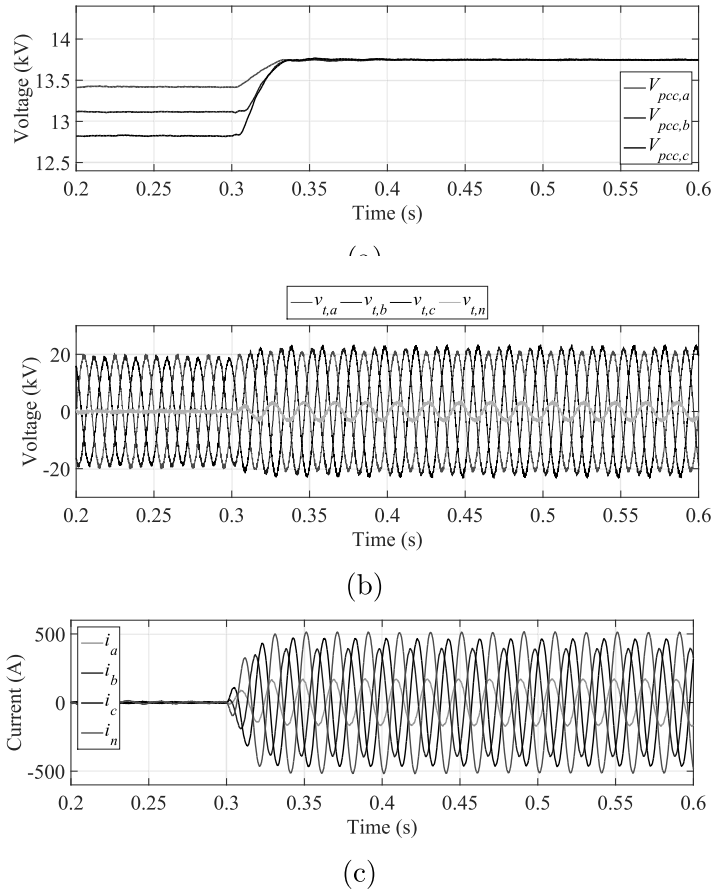
4.3.4 **Case 3**

In this last case, the magnitude of the positive-sequence voltage is less than 24 kV and the PCC voltages are unbalanced due to a presence of a zero-sequence voltage component. Figures 58 (a), (b) and (c) show the RMS values of the PCC voltages and the waveforms of MMC-STATCOM terminal voltages and currents, respectively. From $t = 0.2$ s to $t = 0.3$ s the positive-sequence voltages at the PCC are below the system nominal value and they are also unbalanced due to a zero-sequence voltage component. At $t = 0.3$ s the MMC-STATCOM starts synthesizing currents at its terminals in order to regulate the positive-sequence voltage at the system nominal value (24 kV) and to compensate the zero-sequence voltage at the PCC.

Figures 59 (a) and (b) show the SM voltages of the upper and lower arms of the phase "a" and the fourth-leg of the MMC-STATCOM, respectively. It can be noted that the DC voltages are regulated simultaneously with the two others strategies of voltage compensation.

Ideally, when a three-wire three-phase MMC is used for reactive power compensation or harmonic filtering and also considering that the circulating currents compensation is performed in the natural coordinates, there is no need to compensate the circulating currents of all three legs of the converter. Therefore, in this case, it is enough to compensate the circulating currents of two converter's legs since there will be no DC component in the

Figure 58 – Waveforms of the PCC voltages and static compensator terminal voltages and currents for the Case 3 in which the 3-phase 4-wire MMC-STATCOM regulates the positive- and zero-sequence voltages at the PCC.



Caption: (a) RMS values of the PCC voltages, (b) MMC-STATCOM terminal voltages and (c) MMC-STATCOM terminal currents.

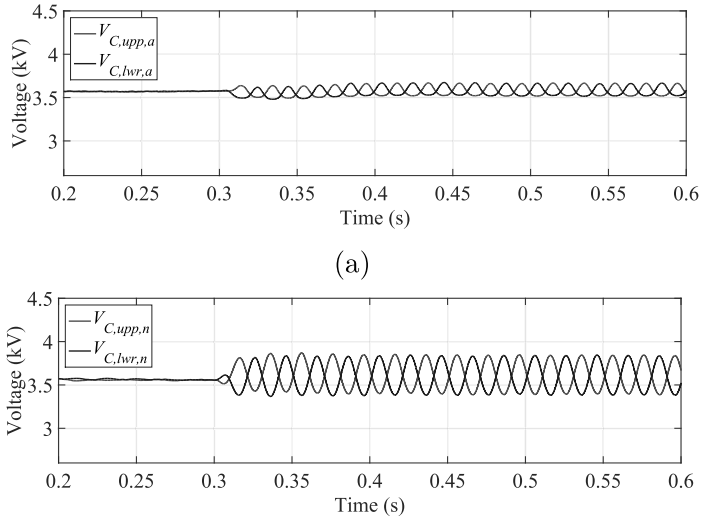
Source: Elaborated by the author (2021).

circulating current (see Subection 3.2.6).

Thus, without loss of generality, for the three-phase four-wire MMC-STATCOM, assuming that all the converter's legs have the same impedance, the compensation of the circulating currents can be performed by regulating only the currents of three legs of the converter. This assertion is reinforced by the fact that the three-phase four-wire MMC-STATCOM can be viewed as three-leg converter in the synchronous reference frame. Then, the compensation of the circulating current can be performed only regulating $I_{cir,d2}$ and $I_{cir,q2}$, as shown in Diagram 23.

Figures 60 (a) and (b) show the circulating currents of phase "a" and neutral legs of the three-phase four-wire MMC-STATCOM, respectively, considering the operation with and without the controller designed in Subection 3.2.6. It can be noted that by controlling only the circulating currents of the phases "a", "b" and "c" the circulating

Figure 59 – Waveforms of the static compensator DC voltages for the Case 3 in which the 3-phase 4-wire MMC-STATCOM regulates the positive- and zero-sequence voltages at the PCC.



(a)

(b)

Caption: (a) upper and lower arm SM capacitor DC voltages of phase "a" and (b) upper and lower arm SM capacitor DC voltages of neutral.

Source: Elaborated by the author (2021).

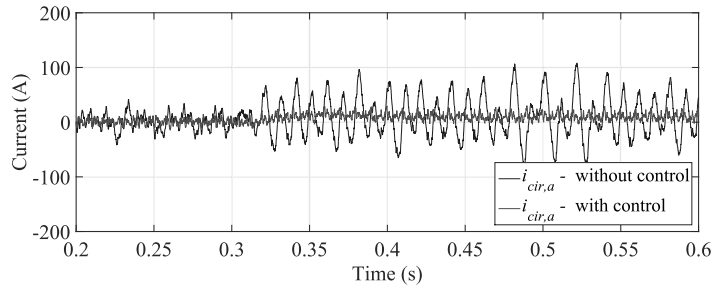
current through the MMC-STATCOM's neutral leg is also controlled.

In the next chapter it will be shown both strategies of negative- and zero-sequence voltage compensation at the PCC working simultaneously.

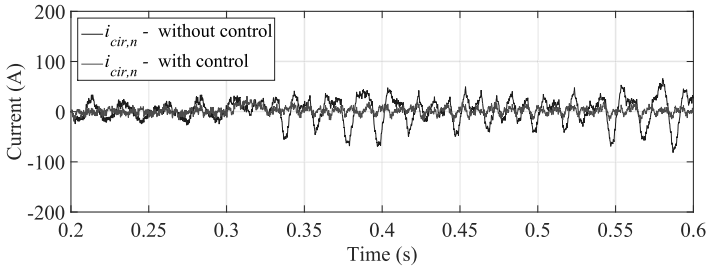
4.4 CONCLUSIONS

This chapter presented a zero-sequence network voltage compensation strategy to control a three-phase four-wire static synchronous compensator based MMC. A mathematical modelling of the static compensator was presented in the Section 3.2 in order to control the positive-sequence voltage at the point of common coupling. The developed model allowed to design positive-sequence voltage and current control loops for the static compensator. Furthermore, the controllers parameters could be chosen according to the design methodology presented. On the other hand, in this chapter, the SOGI and buffer circuits allowed to transform the zero-sequence voltage and current, respectively, to a fictitious synchronous reference frame. Then, the zero-sequence PCC voltage and MMC-STATCOM terminal current could be controlled in a manner similar to the strategy developed to control the positive-sequence quantities. Moreover, the same design methodology used for the positive-sequence controllers could be used for the zero-sequence controllers. Again, a first-order low-pass filter was connected to the feedback of the DC

Figure 60 – Waveforms of the static compensator circulating currents for the Case 3 in which the 3-phase 4-wire MMC-STATCOM regulates the positive- and zero-sequence voltages at the PCC.



(a)



(b)

Caption: (a) phase "a" and (b) neutral.

Source: Elaborated by the author (2021).

voltage control loop in order to mitigate the commutation harmonics in the measured DC voltage. Results of digital simulations were presented to validate the mathematical analysis and to demonstrate the performance of the voltage and current control strategies. It was shown that the static compensator can synthesize positive- and zero-sequence currents to regulate and compensate the positive- and zero-sequence voltages at the PCC, respectively. The static compensator's leg connected to the neutral should be designed to synthesize a current three times greater than the phase currents. Furthermore, it was shown that the SM DC voltages of the static compensator were regulated simultaneously with both positive- and zero-sequence voltage compensation strategies.

5 CONTROL ALGORITHM FOR STATCOM TO COMPENSATE CONSUMER-GENERATED NEGATIVE- AND ZERO-SEQUENCE VOLTAGE UNBALANCE

This chapter presents the control strategy proposed in (DUARTE *et al.*, 2020a) and (DUARTE *et al.*, 2020b). A consumer unbalance assessment methodology, developed in the time domain, is used to generate the reference signals for the negative- and zero-sequence voltage control loops of the MMC-STATCOM so that only the voltage unbalance at the PCC caused by the consumer will be compensated.

5.1 INTRODUCTION

A topic that has been very discussed in conferences and forums around the word is the power quality responsibility. Engineers and researches have been discussing and proposing criteria to penalize consumers who are responsible for compromising the power quality of the electric networks (XU; LIU, 2000; SHOJAIE; MOKHTARI, 2014). Although several studies presented in the literature focus on issues related to harmonic pollution (XU; LIU, 2000), the development of methodologies capable of quantifying the responsibilities of the supplier and the consumer in the system's power quality indexes, such as the voltage unbalance, is essential (GREGORY; SCOTTI; OLIVEIRA, 2018a).

The works (JAYATUNGA *et al.*, 2015a; JAYATUNGA *et al.*, 2015b; SUN; XIE; LI, 2018; ABASI *et al.*, 2018) are based on the methodology proposed by IEC (IEC, 2008) to determine the unbalance responsibility, or in an improved variation of it. A Voltage Unbalance Factor (VUF), defined as the ratio between the negative- and positive-sequence voltages at the PCC and measured before and after the load is connected, is used to quantify the responsibility for the system's unbalance. Although simpler, this methodology presents problems related to the intermittence of the loads, and also faces difficulties in recognizing pre and post load connection conditions, as well as measuring the voltages and currents in each previous condition. All these issues increase the complexity of time-domain algorithm implementation.

In (SEIPHETLHO; RENS, 2010), a three-phase power flow tool is used to detect the direction of the negative-sequence flow. The method decomposes the voltages and currents at the load bus by means of symmetrical components. Then, it calculates the active power due to the negative-sequence components, for each load, in order to identify the individual responsibility parcels. However, as shown in (ARÃO; FILHO; MENDONÇA, 2015), this method may produce inconsistent results depending on the system's configuration.

Another method proposed in the literature defines the parcels of responsibility of the electric utility (supplier) and consumer (load) based on conforming and non-conforming currents (SRINIVASAN; JUTRAS, 1998). The sum of these two currents is assumed

to be equal to the current drained by the load while the conforming current is defined as the parcel of the current that is proportional to the voltage at the PCC. Thus, the non-conforming current will be the difference between the current drained by the load and the conforming one. Based on this, the proposed method infers that the conforming and non-conforming currents are related to the responsibilities of the supplier and consumer, respectively. Nevertheless, this methodology may present inconsistent results when applied with dynamic loads *e.g.* induction and synchronous machines, due to the small difference between the positive- and negative-sequence impedances.

In (SUN *et al.*, 2017), the authors propose a method based on (ARÃO; FILHO; MENDONÇA, 2015) to determine the individual contribution of various sources of unbalance in a power system. In addition to using the voltage and current values measured at the PCC, the authors propose a method for estimating the negative-sequence component in each feeder using the aggregate load impedance concept. As in the previous work, in (YANG; WANG; MA, 2019) it is presented an algorithm also capable of making this estimation. However, neither of these works use a time-domain approach to perform their task.

All of the above mentioned methods were experimentally compared in (ARÃO; FILHO; MENDONÇA, 2015) and (GREGORY; SCOTTI; OLIVEIRA, 2018b). The analysis of the results showed that the methodology based on conforming and non-conforming currents is the best option to identify the imbalance responsibilities when the consumer has static loads. However, it is fundamental to establish a method capable of quantifying, in the time domain, the parcels of voltage imbalance responsibility between the electric utility and the consumer.

Thus, another objective of this work is to present a methodology to quantify, in the time-domain, the voltage imbalance parcels at the PCC due to the utility system (supplier) as well as the one due to the consumer (load). The methodology presented in this chapter will be used to control a MMC-STATCOM to compensate only the voltage unbalance generated by the consumer, avoiding the compensation of all the negative- and zero-sequence voltages at the PCC. Results of digital simulations of the MMC-STATCOM connected to an unbalanced distribution system, based on a modification in the IEEE 13-bus system, are used to validate the methodology of voltage imbalance responsibility.

5.2 VOLTAGE IMBALANCE RESPONSIBILITY METHODOLOGY

The methodology of voltage unbalance responsibility presented in this chapter is based on the methodology proposed in (XU; LIU, 2000) to quantify the harmonic distortion caused by a non-linear load connected to a power system. However, unlike the original methodology, the method presented here does not require measurements to be made on the network prior to consumer connection and, as will be shown below, it will

only require knowledge of the equivalent system and consumer impedance values at the PCC (GREGORY; SCOTTI; OLIVEIRA, 2018a). In practice these impedances can be estimated using different methods (MONTEIRO, 2018).

Different from the other chapters of this thesis, for the sake of simplicity, the methodology presented in this chapter will be developed in the natural coordinates. Diagram 32 (a) shows the equivalent Norton circuit, in the frequency domain, for the supplier and consumer. This circuit can be decomposed into the equivalent circuits of Diagram 32 (b) and Diagram 32 (c), where the supplier and consumer contributions for the negative-sequence current at the PCC are highlighted.

Having in mind the circuit of Diagram 32 (a) the following relation can be written:

$$I_{l,2}(s) = \frac{V_{pcc,2}(s)}{Z_{l,2}\,(s)} - I_{pcc,2}(s), \tag{5.1}$$

where $I_{l,2}(s)$ is the negative-sequence current of the consumer (load), $V_{pcc,2}(s)$ and $I_{pcc,2}(s)$ are the negative-sequence voltage and current at the PCC, respectively, and $Z_{l,2}\,(s) = (R_{l,2} + sL_{l,2})$ is the negative-sequence equivalent impedance of the consumer (load) seen from the PCC.

Now, from the circuit of Diagram 32 (c) the following relations can be written for the consumer's voltage and current at the PCC:

$$V_{pcc,2,l}(s) = -Z_{s,2}\,(s)\, I_{pcc,2,l}(s) \tag{5.2}$$

and

$$I_{l,2}(s) = \frac{V_{pcc,2,l}(s)}{Z_{l,2}\,(s)} - I_{pcc,2,l}(s), \tag{5.3}$$

where $V_{pcc,2,l}(s)$ and $I_{pcc,2,l}(s)$ are the consumer's (load) contribution for the negative-sequence voltage and current at the PCC, respectively, and $Z_{s,2}\,(s) = (R_{s,2} + sL_{s,2})$ is the negative-sequence equivalent impedance of the supplier seen from the PCC.

The substitution of (5.1) and (5.2) into (5.3) yields:

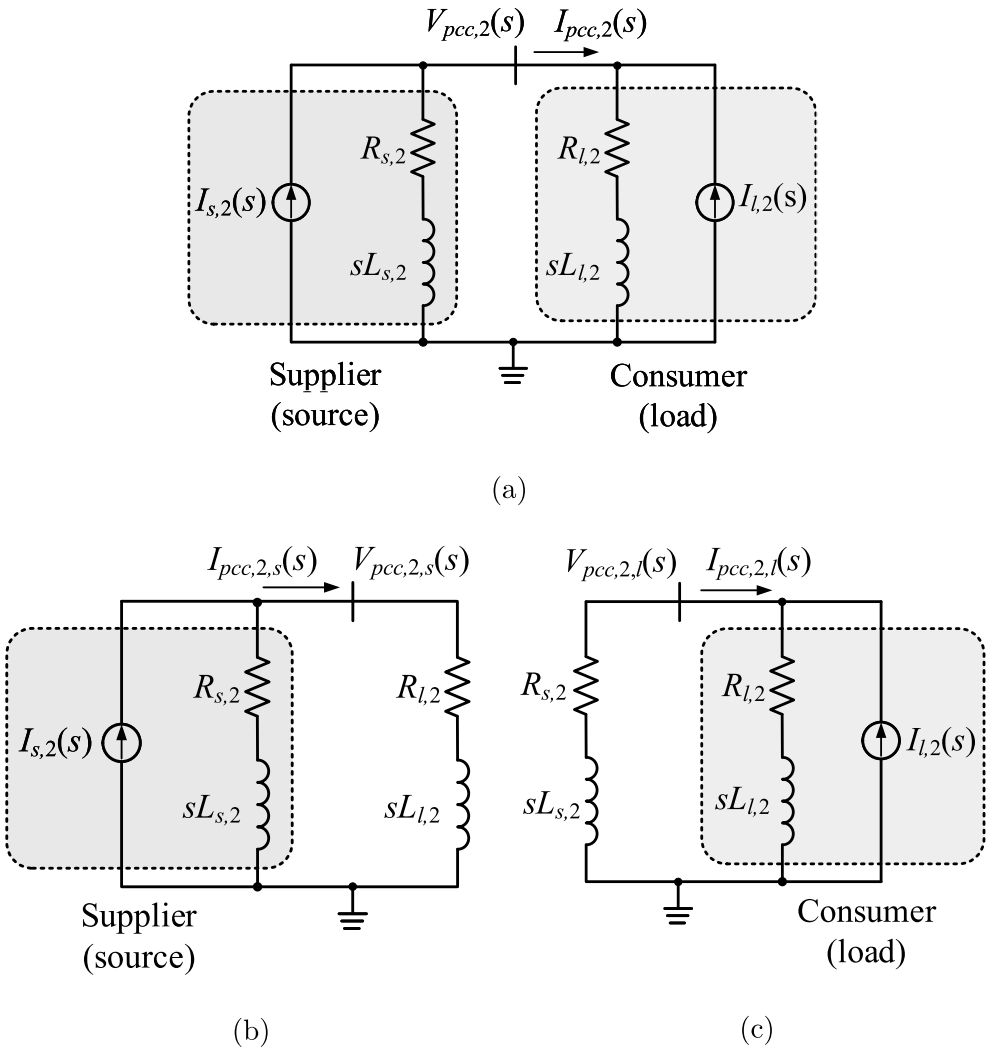
$$\frac{V_{pcc,2}(s)}{Z_{l,2}\,(s)} - I_{pcc,2}(s) = -\left[\frac{Z_{s,2}\,(s)}{Z_{l,2}\,(s)} + 1\right] I_{pcc,2,l}(s). \tag{5.4}$$

Manipulating (5.4) the following expression is obtained:

$$I_{pcc,2,l}(s) = -\left(\frac{1}{Z_{s,2}\,(s) + Z_{l,2}\,(s)}\right) V_{pcc,2}(s) + \left(\frac{Z_{l,2}\,(s)}{Z_{s,2}\,(s) + Z_{l,2}\,(s)}\right) I_{pcc,2}(s). \tag{5.5}$$

Then, knowing the values of the equivalent impedances $Z_{s,2}$ and $Z_{c,2}$, the consumer's contribution for the negative-sequence current at the PCC can be determined by (5.5) measuring the negative-sequence voltage and current at the PCC. As already commented, when these parameters are not known, different methods can be used to estimate the grid and consumer impedances, as shown in (MONTEIRO, 2018).

Diagram 32 – Equivalent Norton circuits for the voltage unbalance responsibility methodology.



Caption: (a) negative-sequence equivalent circuit, (b) contribution of the supplier for the current at the PCC and (c) contribution of the consumer for the current at the PCC.

Source: Reproduced from (DUARTE *et al.*, 2020a).

5.3 TRANSFORMATION OF THE VOLTAGE UNBALANCE ASSESSMENT TO THE TIME DOMAIN

Applying the inverse Laplace transform in (5.5) and rearranging the resulting expression, the following relation can be written in the time domain:

$$\frac{di_{pcc,2,l}}{dt} = -\left(\frac{R_{t,2}}{L_{t,2}}\right) i_{pcc,2,l} + \left(\frac{R_{l,2}}{L_{t,2}}\right) i_{pcc,2} + \left(\frac{L_{l,2}}{L_{t,2}}\right) \frac{di_{pcc,2}}{dt} - \left(\frac{1}{L_{t,2}}\right) v_{pcc,2}, \tag{5.6}$$

being $R_{t,2} = (R_{s,2} + R_{l,2})$, $L_{t,2} = (L_{s,2} + L_{l,2})$ and the lower case letters v and i used to

represent the voltages and currents in the time domain, respectively.

After realizing a variable substitution, (5.6) can be rewritten by:

$$\frac{d\xi_2}{dt} = -\left(\frac{R_{t,2}}{L_{t,2}}\right)\xi_2 - \left(\frac{1}{L_{t,2}}\right)v_{pcc,2} + \left(\frac{R_{l,2}L_{t,2} - R_{t,2}L_{l,2}}{(L_{t,2})^2}\right)i_{pcc,2}, \tag{5.7}$$

where $\xi_2 = i_{pcc,2,l} - (L_{l,2}/L_{t,2})\, i_{pcc,2}$.

The expression (5.7) can be rewritten in the form of state space as follows:

$$\begin{cases} \dot{x_2} = A_2 x_2 + B_2 u_2 \\ y_2 = C_2 x_2 + D_2 u_2 \end{cases}, \tag{5.8}$$

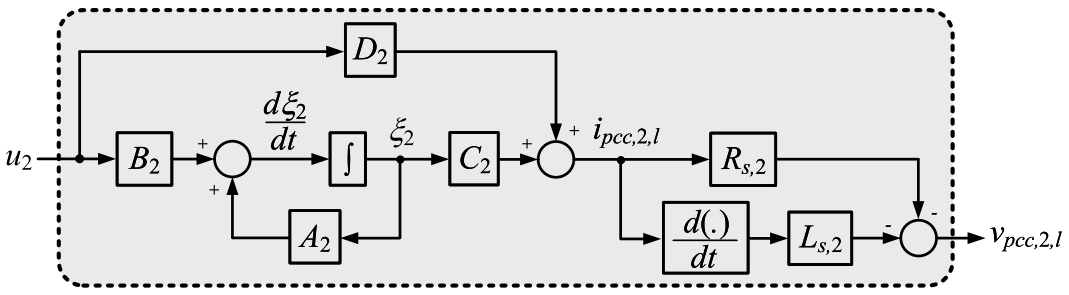
where $A_2 = \left[\frac{-R_{t,2}}{L_{t,2}}\right]$, $B_2 = \left[\begin{array}{cc} \frac{R_{l,2}L_{t,2}-R_{t,2}L_{l,2}}{(L_{t,2})^2} & \frac{-1}{L_{t,2}} \end{array}\right]$, $C_2 = 1$, $D_2 = \left[\begin{array}{cc} \frac{L_{l,2}}{L_{t,2}} & 0 \end{array}\right]$, $x_2 = \xi_2$, $y_2 = i_{pcc,2,l}$, $u_2 = \left[\begin{array}{cc} i_{pcc,2} & v_{pcc,2} \end{array}\right]^t$, being the superscript t used to represent the transposed vector.

Solving (5.7)–(5.8) for $y_2 = i_{pcc,2,l}$, and rewritten the expression (5.2) in the time domain, the consumer's contribution for the negative-sequence voltage at the PCC is calculated by:

$$v_{pcc,2,l} = -L_{s,2}\frac{di_{pcc,2,l}}{dt} - R_{s,2}i_{pcc,2,l}. \tag{5.9}$$

Diagram 33 shows the block diagram of the algorithm used to quantify, in real time, the consumer responsibility parcel for the negative-sequence imbalance at the PCC. It can be noted that the consumer's contribution for the negative-sequence voltage is calculated using the measured values of voltage and current at the PCC. Furthermore, the use of the derivation block of Diagram 33 must be used with care in practice, since the input signal can present noise. However, in this case, some artifices can be used to workaround this drawback (FOGLI, 2018).

Diagram 33 – State space block diagram for the algorithm used to compute in real time the negative-sequence voltage caused by the consumer.



Source: Reproduced from (DUARTE *et al.*, 2020a).

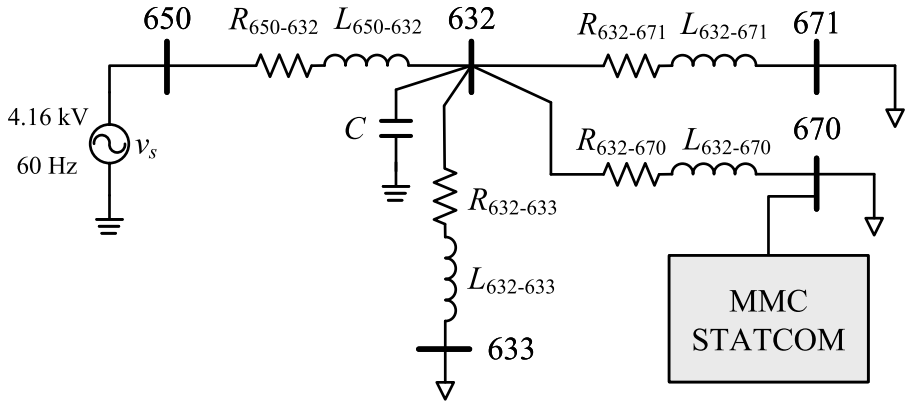
The dynamic equations presented in this section can be easily incorporated into the MMC-STATCOM's controller in order to compensate the negative-sequence voltage

unbalance caused by a consumer connected to the PCC. Moreover, following the same steps made to derive the negative-sequence voltage imbalance estimator, it is possible to build a block diagram similar to that shown in Diagram 33, to estimate the consumer-generated zero-sequence voltage unbalance at the PCC. This algorithm can also be incorporated into the MMC-STATCOM's controller.

5.4 DIGITAL SIMULATION OF THE CONSUMER'S VOLTAGE IMBALANCE ASSESSMENT ALGORITHM

Diagram 34 shows the single-line diagram of an unbalanced distribution system, with 5 nodes, modelled in an electromagnetic transient program. This system is based on a modification of the IEEE 13-bus system, where a MMC-STATCOM with all its controllers was modelled and connected to the bus 670. The IEEE 13-bus system was modified by using a method to reduce the circuit to an equivalent circuit with less nodes (DUARTE *et al.*, 2020a; DUARTE *et al.*, 2020b). Tables 11, 12 , 13 and 14 (Appendix B) show the parameters of the electric network, MMC-STATCOM, digital filters and controller gains of the MMC-STATCOM, respectively. Tables 15, 16 and 17 (Appendix B) show the parameters of the loads, capacitor bank and feeders of the 4.16 kV 5-bus system of Diagram 34, respectively. The positive-, negative- and zero-sequence equivalent impedances of the circuit of Diagram 34, used in the PCC voltage controllers of the MMC-STATCOM and in the consumer's voltage imbalance assessment algorithm, were calculated based on the nodal admittance matrix of the electrical system.

Diagram 34 – Single-line diagram of the 5-bus distribution network with the MMC-STATCOM connected to the bus 670.



Source: Reproduced from (DUARTE *et al.*, 2020a).

A Phase-Locked Loop based on Dual Second-Order Generalized Integrator (DSOGI-PLL) synchronizes the voltages and currents at the MMC-STATCOM terminals with the PCC voltages (RODRIGUEZ *et al.*, 2006). A PD-PWM technique is used to generate the switching pattern for the IGBTs of the static compensator. The voltages of the upper

and lower arm SMs are regulated using an algorithm that measures and sorts the SMs in descending order according to their DC voltages, as proposed in (GHETTI *et al.*, 2017).

Two distinct cases were simulated in order to validate the selective compensation of the negative- and zero-sequence voltages at the PCC: (*i*) compensation of all voltage imbalance at the PCC and (*ii*) compensation of only the parcel of voltage imbalance at the PCC caused by the consumer (load) connected to the bus 670. In all cases, the circulating current control of the MMC-STATCOM is active.

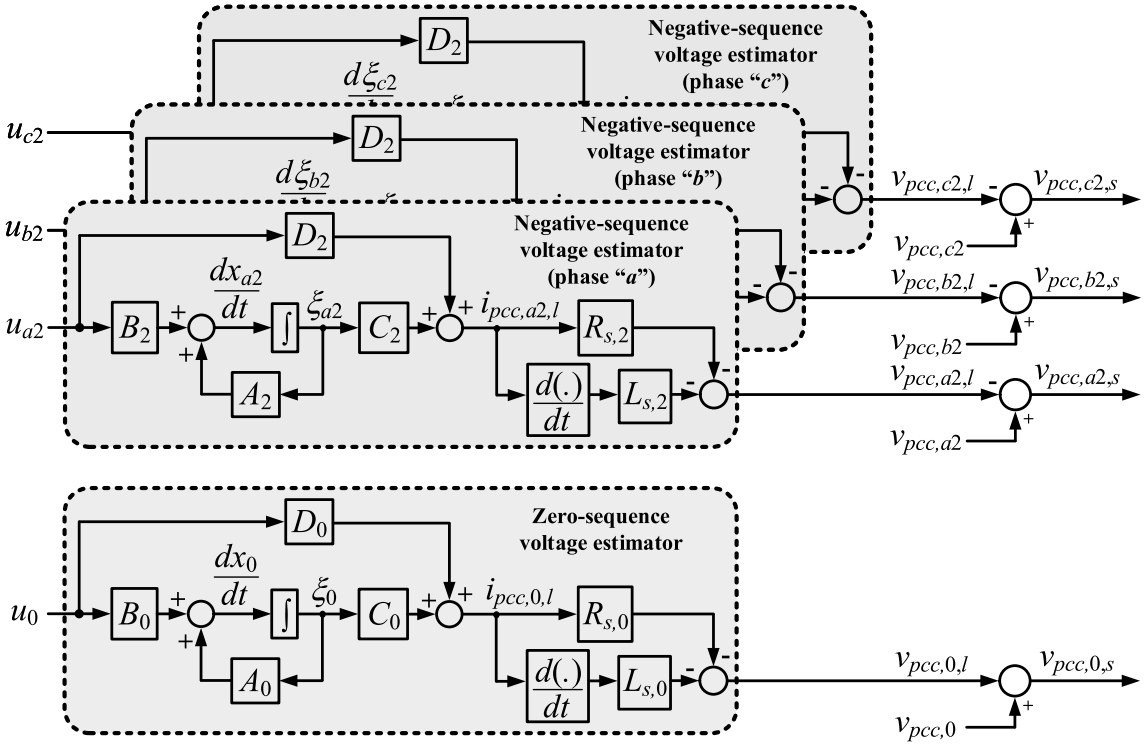
In the first case the MMC-STATCOM compensates for all the zero- and negative-sequence voltages at the PCC. Figures 61 (a), (b), (c), (d) and (e) show the waveforms of the currents of the consumer, the RMS voltages at the PCC, the negative-sequence voltage at the PCC, the zero-sequence voltage at the PCC and the VUFs for the PCC voltages, respectively. Figures 63 (a) and (b) show the AC terminal currents and voltages of the MMC-STATCOM, respectively. On the other hand, Figures 65 (a), (b), (c) and (d) show the waveforms of the DC capacitor voltages of the phase "*a*" upper and lower arm SMs, the DC capacitor voltages of the neutral upper and lower arm SMs, the upper arm SMs DC capacitor voltages of the three-phases and the three-phase circulating currents, respectively.

In the second case the MMC-STATCOM compensates for only the parcel of the zero- and negative-sequence voltage caused by the load connected to the bus 670. Diagram 35 shows the block diagram of the algorithm used to compute the references for the negative- and zero-sequence voltage controllers of the MMC-STATCOM (see Diagram 21 and Diagram 30). The zero- and negative-sequence voltages and currents measured at the PCC are used to extract the parcels of imbalance caused by the consumer by using the algorithms of voltage unbalance estimation of Diagram 35. The output signals of these estimators are subtracted from the negative- and zero-sequence voltages at the PCC and, after be transformed to the synchronous coordinates, they are sent as reference signals for the MMC-STATCOM's voltage controllers of Diagram 21 and Diagram 30, respectively. Figure 62, Figure 64 and Figure 66 show the same waveforms of Figure 61, Figure 63 and Figure 65, respectively.

At t = 0.4 s the MMC-STATCOM starts synthesizing currents to compensate for the unbalanced voltages at the PCC. In the first case the MMC-STATCOM synthesizes three-phase currents of the order of 150 A (peak) in order to compensate for all the negative- and zero-sequence voltage at the PCC. On the other hand, in the second case the MMC-STATCOM synthesizes three-phase currents much lower (75 A of peak) compared to the previous case. It is possible also to note that, different from the first case where the voltage imbalance at the PCC is completely eliminated, in the second case the zero- and negative-sequence voltages at the PCC are not fully compensated.

Another interesting conclusion is derived from the comparison of Figure 65 and

Diagram 35 – Block diagram for the algorithm used to calculate the references for the MMC-STATCOM voltage controllers.



Source: Reproduced from (DUARTE *et al.*, 2020a).

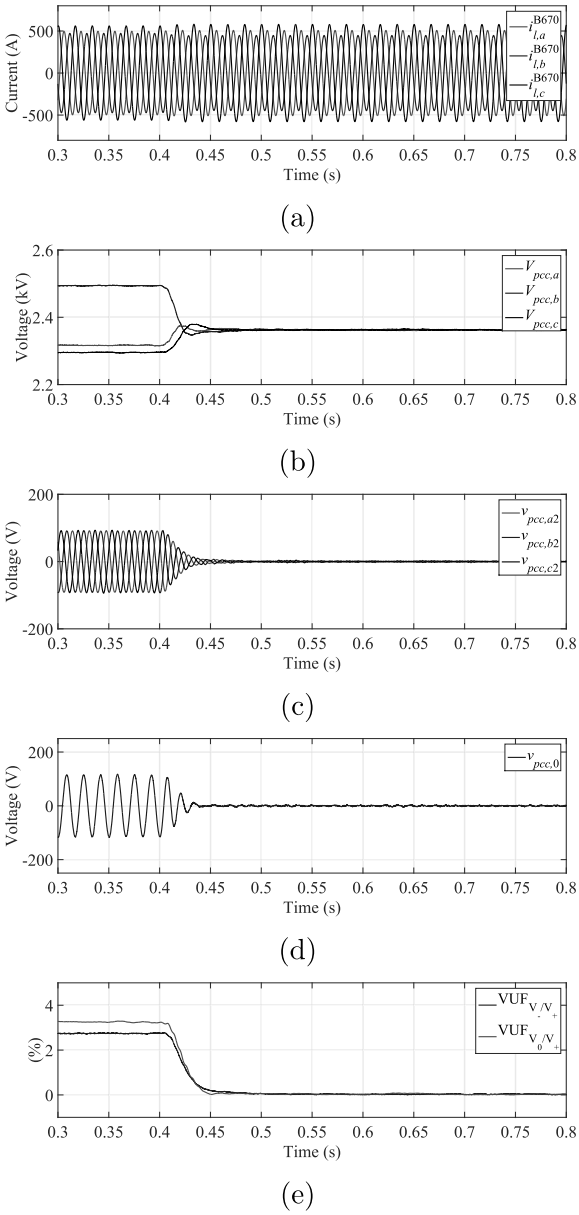
Figure 66. Since the MMC-STATCOM compensates for only the consumer-generated imbalance in the second case, the oscillation in the voltages of the DC capacitors is much lower compared to the first case. Furthermore, it can be noted in Figure 65 (d) and Figure 66 (d) that the controller of the MMC-STATCOM fully compensates the second harmonic of the circulating currents.

5.4.1 Performance of the consumer imbalance estimator under uncertainties of grid or load impedance

As the parameters of the grid and consumer vary all the time, this subsection investigates the performance of the consumer's imbalance assessment algorithm when the estimated values Z_s^e or Z_c^e used in the Diagram 35 are different from the actual values of the grid and load impedances, respectively.

Figure 67 (a) shows the RMS value of the negative-sequence voltage while Figure 67 (b) shows the RMS value of the zero-sequence voltage, both measured at the PCC, when the estimated grid impedance Z_s^e varies in the range of $\pm$ 30% of the actual value of Z_s. At $t = 0.4$ s the MMC-STATCOM starts to compensate for the consumer-generated imbalance at the PCC. It is possible to perceive that there are no significant discrepancies in the negative- and zero-sequence values of the compensated voltages for $Z_s^e = (Z_s - 0.3Z_s)$,

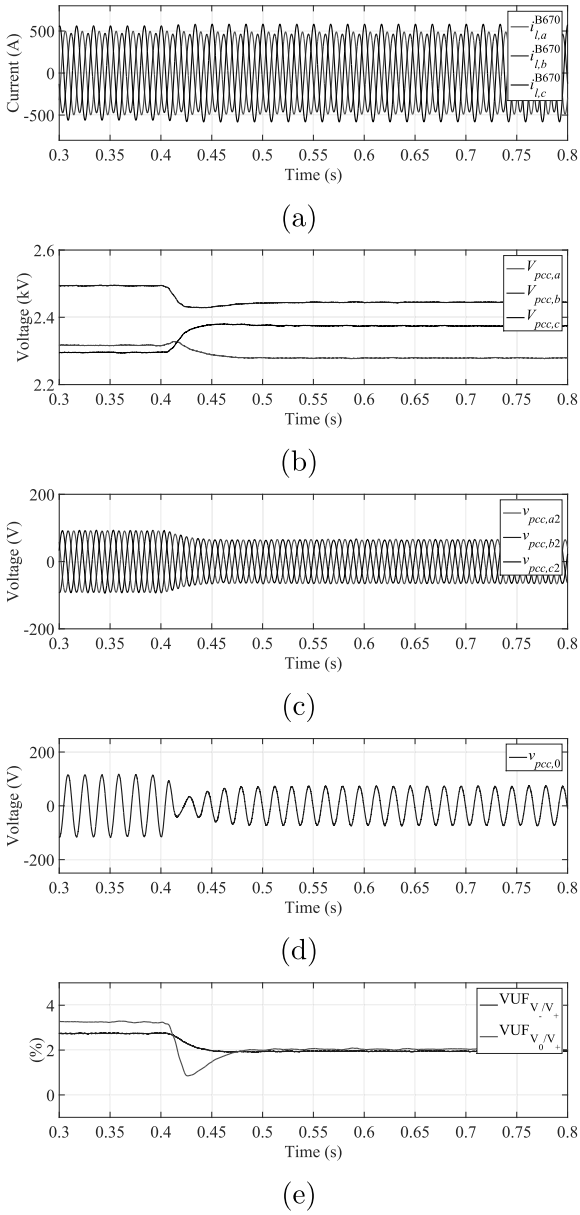
Figure 61 – Waveforms of the electric network for the Case 1.



Caption: (a) currents of the consumer, (b) RMS voltages at the PCC, (c) negative-sequence voltages at the PCC, (d) zero-sequence voltage at the PCC and (e) voltage unbalance factors.

Source: Elaborated by the author (2021).

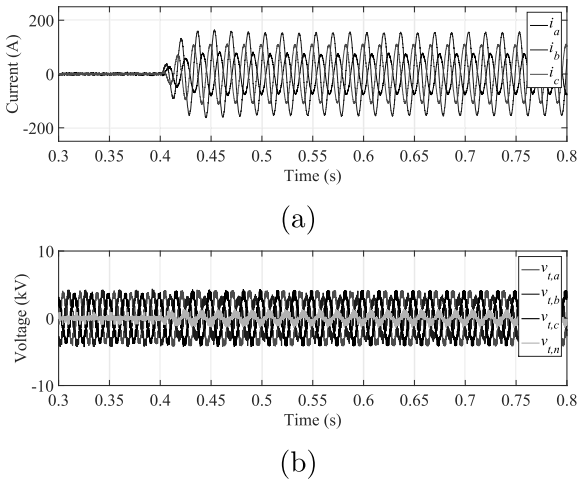
Figure 62 – Waveforms of the electric network for the Case 2.



Caption: (a) currents of the consumer, (b) RMS voltages at the PCC, (c) negative-sequence voltages at the PCC, (d) zero-sequence voltage at the PCC and (e) voltage unbalance factors.

Source: Elaborated by the author (2021).

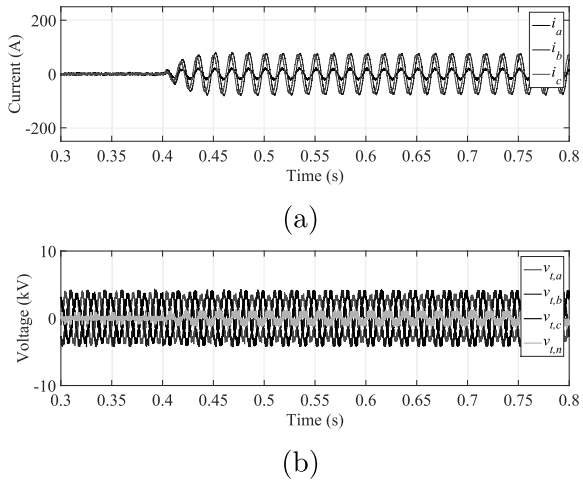
Figure 63 – Waveforms of the MMC-STATCOM terminal currents and voltages for the Case 1.



Caption: (a) currents and (b) voltages.

Source: Elaborated by the author (2021).

Figure 64 – Waveforms of the MMC-STATCOM terminal currents and voltages for the Case 2.



Caption: (a) currents and (b) voltages.

Source: Elaborated by the author (2021).

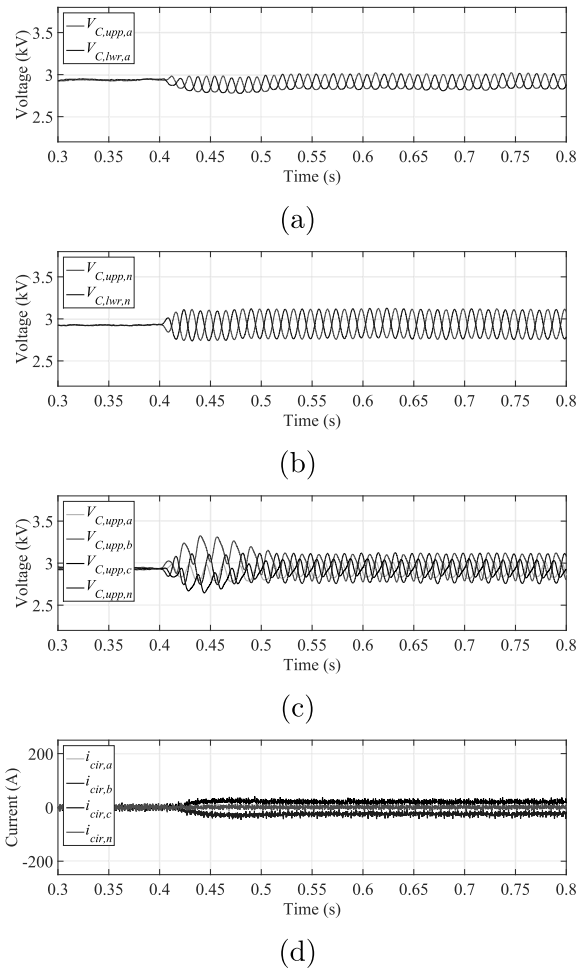
$Z_s^e = Z_s$, and $Z_s^e = (Z_s + 0.3Z_s)$.

Figures 68 (a) and (b) show the RMS values of the negative- and zero-sequence voltages measured at the PCC when the estimated impedance Z_c^e is varied between $(Z_c - 0.3Z_c)$, Z_c, and $(Z_c + 0.3Z_c)$. Unlike the previous case, the consumer-generated imbalance estimator produces errors when $Z_c^e \neq Z_c$. Fortunately, when $Z_c^e < Z_c$, the MMC-STATCOM compensates for a slightly larger unbalance than that one caused by the consumer. In this scenario, considering $Z_c^e = (Z_c - 0.3Z_c)$, the errors in the negative- and zero-sequence RMS voltages measured at the PCC after being compensated by the MMC-STATCOM will be approximately 3% and 7%, respectively. On the other hand, when $Z_c^e > Z_c$, the estimation algorithm will force the MMC-STATCOM to compensate a smaller unbalance than the one generated by the consumer at the PCC. An alternative to overcome the aforementioned problem can be achieved by using an on-line strategy or algorithm to scan the value of the consumer impedance as shown in (MONTEIRO, 2018). As this issue is not the aims of this work it will not be investigated.

5.5 CONCLUSIONS

This chapter presented a methodology to estimate the parcels of voltage unbalance responsibility related to the supplier and consumer in a distribution network. The proposed methodology is used to calculate, in real time, the negative- and zero-sequence voltage at the PCC caused by the consumer. The methodology presented was used to derive a control algorithm, based on the consumer-generated voltage unbalance assessment, to generate

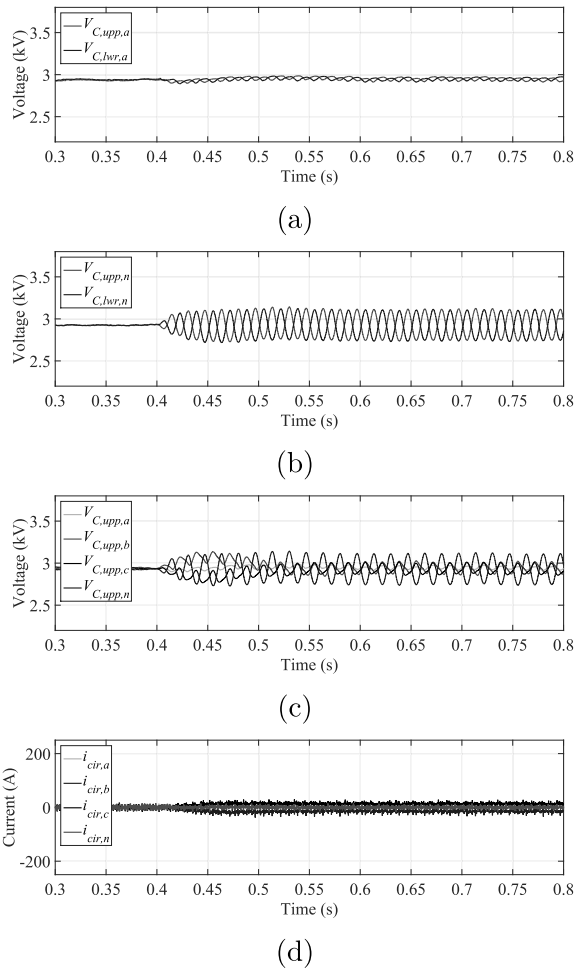
Figure 65 – Waveforms of the MMC-STATCOM DC capacitors and circulating currents for the Case 1.



Caption: (a) upper and lower arm SM DC capacitor voltages of phase "a", (b) upper and lower arm SM DC capacitor voltages of neutral, (c) upper arm SM DC capacitor voltages of the three phases and (d) circulating currents.

Source: Elaborated by the author (2021).

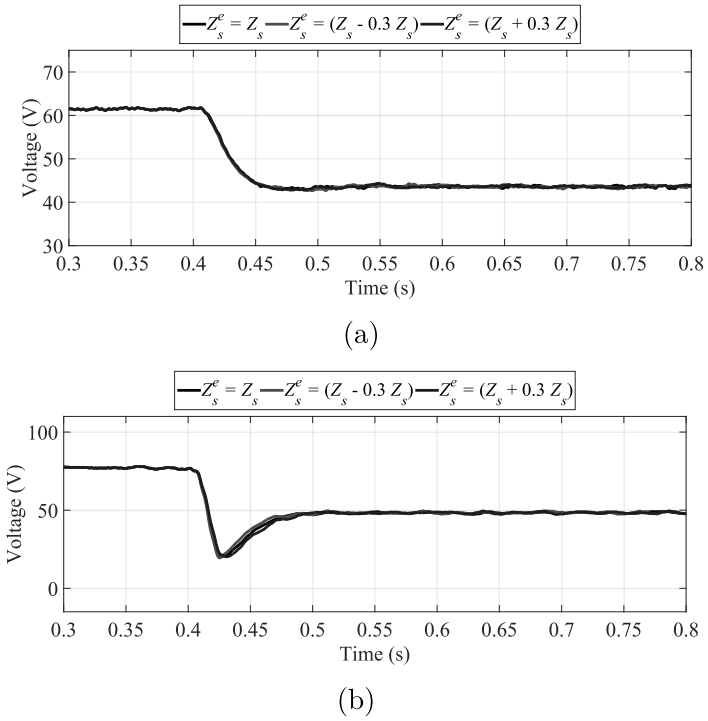
Figure 66 – Waveforms of the MMC-STATCOM DC capacitors and circulating currents for the Case 2.



Caption: (a) upper and lower arm SM DC capacitor voltages of phase "a", (b) upper and lower arm SM DC capacitor voltages of neutral, (c) upper arm SM DC capacitor voltages of the three phases and (d) circulating currents.

Source: Elaborated by the author (2021).

Figure 67 – Behaviour of the RMS voltage at the PCC for variations in the estimated supplier impedance.

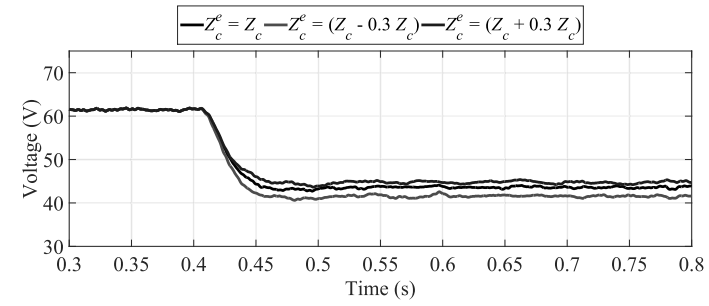


Caption: (a) negative-sequence and (b) zero-sequence.

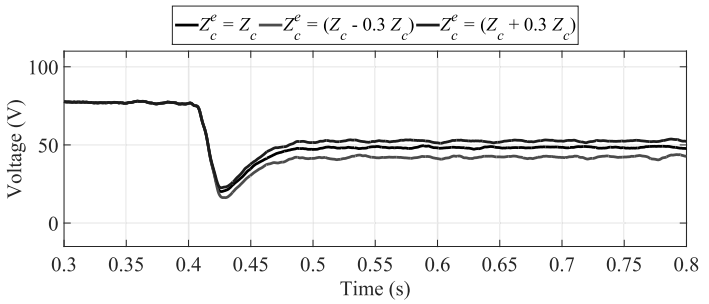
Source: Elaborated by the author (2021).

the reference signals to control the MMC-STATCOM in order to compensate for only the negative- and zero-sequence voltage at the PCC caused by the consumer. Results of digital simulations were also presented to demonstrate the methodology used to calculate, in the time-domain, the imbalance generated by the consumer. The obtained results shows that the ratings of the static compensator is much smaller when it is designed to compensate for only the parcel of voltage imbalance caused by the consumer. Moreover, the possible financial penalties due to the imbalances caused by the consumer would be avoided.

Figure 68 – Behaviour of the RMS voltage at the PCC for variations in the estimated consumer impedance.



(a)



(b)

Caption: (a) negative-sequence and (b) zero-sequence.

Source: Elaborated by the author (2021).

6 FINAL CONCLUSIONS

This work presented some contributions to the operation and control of three-phase three-wire and three-phase four-wire static synchronous compensators based on modular multilevel converter. An energizing strategy was presented for the static compensator, in which no additional current limiting resistors, inductors, transformers, auxiliary DC sources and mechanical switches were used. Instead, two thyristors were parallel connected to the mechanical switch used to connect the static compensator to the electric network in order to control the energizing current drained by the DC capacitors of the submodules. This is one of the contributions of this work, since the energizing strategy presented in most of the works in the literature only limits the energizing current at the initial instants, when the DC capacitors are fully discharged. Moreover, it was shown that the power dissipated by the thyristors is of the order of a thousand times lower when it is compared to the power dissipated when a bank of resistors are used to limit the energizing current of the MMC-STATCOM. In addition to that, it was shown that simple modifications in the presented energizing strategy allows also to energize a three-phase four-wire static synchronous compensator.

A negative-sequence network voltage compensation strategy, by using a three-phase three-wire MMC-STATCOM, was also presented. Although there are works in the literature were static converters are used for voltage regulation and compensation in power systems, a mathematical model for the negative-sequence voltage compensation at the point of common coupling is not presented, and consequently, the gains of the compensator's controllers can not be designed. Then, small signal mathematical models, in the synchronous reference frame, were developed to allow that the gains of the negative-sequence voltage controllers of the MMC-STATCOM could be designed. Other contributions of this work derives from the analysis of the developed mathematical models. While the direct-axis current was used to control the quadrature-axis voltage at the PCC, the quadrature-axis current was used to control the direct-axis voltage. Moreover, it was shown that the voltage compensation strategy presented is more interesting for distribution networks with low short-circuit power, since the currents synthesized by the static converter will also be low. Likewise, a zero-sequence network voltage compensation strategy was presented, however by using a three-phase four-wire MMC-STATCOM. The fourth-leg of the static compensator was controlled as a single-phase converter. A buffer and a SOGI circuit were used to generate the quadrature voltages and currents to allow the control of the zero-sequence quantities of the static compensator in a fictitious synchronous reference frame. This is another contribution of this work, since the gains of the MMC-STATCOM's zero-sequence voltage and current controllers could be designed by using the same methodology used for the negative-sequence controllers. A digital low-pass filter was used in the feed-back of the DC voltage controller of the MMC-STATCOM in

order to mitigate the oscillation with twice the grid fundamental frequency in the DC terminal voltage due to the unbalanced AC terminal voltages and currents synthesized by the static compensator. Moreover, it was shown that, for the case of three-phase four-wire MMC-STATCOM's, the circulating current control is performed by controlling only the three-phase circulating currents.

Lastly, a voltage imbalance assessment methodology was presented to estimate the responsibilities between the supplier and consumer on the voltage imbalance at the point of common coupling. Although some methodologies presented in the literature deal with imbalances and harmonic pollution responsibility in distribution networks they are not performed in real time. Thus, another contribution of this work is the adaptation of the voltage imbalance responsibility strategy for the time domain and its incorporation in the static compensator's controller. Thus, the parcel of the voltage imbalance responsibility caused by a consumer were calculated in real time to generate the references for the MMC-STATCOM's voltage controllers. It was shown also that the ratings of the static compensator were reduced when compared to the case where the converter compensates for all the voltage imbalance at the point of common coupling.

6.1 FUTURE WORKS

As future works the following topics are presented in order to improve and continue this work:

a) To investigate the voltage ripple of the SM's capacitors to the MMC operating in unbalanced networks;

b) To study the applicability of the MMC to be used as interface circuit between a photovoltaic system and the electric network;

c) To investigate strategies to energize the MMC used to integrate photovoltaic panels;

d) To investigate the use of others topologies for the MMC's submodules;

e) To search for solutions for the drawbacks of the imbalance responsibility algorithm;

f) To investigate the impact of the DC energizing current on the mains' transformers;

g) To investigate the performance of the energizing strategy when the mains voltage present harmonic components;

h) To develop and implement real-time responsibility algorithms to compensate harmonic components in the PCC voltages.

REFERENCES

ABASI, M.; SEIFOSSADAT, S. G.; RAZAZ, M.; MOOSAPOUR, S. S. Determining the contribution of different effective factors to individual voltage unbalance emission in n-bus radial power systems. **International Journal of Electrical Power & Energy Systems**, Elsevier, v. 94, p. 393–404, 2018.

ABILDGAARD, E. N.; MOLINAS, M. Modelling and control of the modular multilevel converter (MMC). **Energy Procedia**, Elsevier, v. 20, p. 227–236, 2012.

ABUD, T.; BORBA, B.; MACIEL, R.; MACHADO, I. d. S.; FORTES, M. Voltage control analysis of photovoltaic inverters using a real brazilian distribution network. In: IEEE. **2017 IEEE 8th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)**. [S.l.], 2017. p. 1–7.

AKAGI, H. Classification, terminology, and application of the modular multilevel cascade converter (MMCC). **IEEE Transactions on Power Electronics**, IEEE, v. 26, n. 11, p. 3119–3130, 2011.

AKAGI, H.; WATANABE, E. H.; AREDES, M. **Instantaneous power theory and applications to power conditioning**. [S.l.]: John Wiley & Sons, 2007. v. 31.

ALLEBROD, S.; HAMERSKI, R.; MARQUARDT, R. New transformerless, scalable modular multilevel converters for HVDC-transmission. In: IEEE. **Power Electronics Specialists Conference, 2008. PESC 2008. IEEE**. [S.l.], 2008. p. 174–179.

ALMEIDA, A. de O. **Controle Desacoplado Entre um Sistema de Transmissão VSC-HVDC e as Turbinas de um Parque Eólico Offshore em Conexão CC Série**. Master Thesis (Electric Engineering) — Universidade Federal de Juiz de Fora, Juiz de Fora, Brasil, 2019.

ALMEIDA, A. O.; GHETTI, F. T.; RIBEIRO, A. S. B.; ALMEIDA, P. M.; BARBOSA, P. G. Circulating currents suppression strategies for modular multilevel converter. In: IEEE. **Power Electronics Conference (COBEP), 2017 Brazilian**. [S.l.], 2017. p. 1–5.

ALMEIDA, P. M.; MONTEIRO, K. M.; BARBOSA, P. G.; DUARTE, J. L.; RIBEIRO, P. F. Improvement of PV grid-tied inverters operation under asymmetrical fault conditions. **Solar Energy**, Elsevier, v. 133, p. 363–371, 2016.

ALMEIDA, P. M. de. **Modelagem e Controle de Conversores Estáticos Fonte de Tensão utilizados em Sistemas de Geração Fotovoltaicos Conectados à Rede Elétrica de Distribuição**. Master Thesis (Electrical Engineering) — Universidade Federal de Juiz de Fora, 2011.

ANSI Standard. For electric power systems and equipment-voltage ratings (60 Hz) - c84.1-2011. **American National Standard Institute**, 2011.

ARÃO, L. F. L.; FILHO, A. F.; MENDONÇA, M. V. B. Comparative evaluation of methods for attributing responsibilities due to voltage unbalance. **IEEE Transactions on Power Delivery**, IEEE, v. 31, n. 2, p. 743–752, 2015.

ARAUJO, L. R.; PENIDO, D. R. R.; CARNEIRO, S.; PEREIRA, J. L. R. A methodology for optimization of unbalanced distribution systems. **IEEE Latin America Transactions**, IEEE, v. 11, n. 5, p. 1182–1189, Sep. 2013.

ARRILLAGA, J.; ARRILLAGA, J. **High voltage direct current transmission**. [S.l.]: Iet, 1998. v. 29.

ARRILLAGA, J.; WATSON, N. R. **Power system harmonics**. [S.l.]: John Wiley & Sons, 2004.

ÅSTRÖM, K. J.; WITTENMARK, B. **Computer-controlled systems: theory and design**. [S.l.]: Courier Corporation, 2013.

BEHROUZIAN, E.; BONGIORNO, M. Investigation of negative-sequence injection capability of cascaded H-bridge converters in star and delta configuration. **IEEE Transactions on Power Electronics**, IEEE, v. 32, n. 2, p. 1675–1683, 2017.

BISSAL, A.; ALI, W. A fast acting precharge control strategy for modular multilevel converters. In: IEEE. **2019 IEEE 13th International Conference on Power Electronics and Drive Systems (PEDS)**. [S.l.], 2019. p. 1–4.

BOLLEN, M. **Understanding power quality problems**. [S.l.]: IEEE Press, 2000.

BRAGA, H. A.; BARBI, I. Conversores estáticos multiníveis–uma revisão. **SBA Controle & Automação**, v. 11, n. 01, p. 20–28, 2000.

BRAGA, M.; DUARTE, S.; ALMEIDA, P.; BARBOSA, P. DC capacitor energization and voltage regulation of a single-phase hibrid filter. In: SOBRAEP. **Brazilian Power Electronics Conference (COBEP)**. [S.l.], 2017.

BUSO, S.; MATTAVELLI, P. Digital control in power electronics. **Synthesis Lectures on Power Electronics**, Morgan & Claypool Publishers, v. 5, n. 1, p. 1–229, 2015.

CHAVES, F. S. **Avaliação técnica do desempenho da compensação reativa shunt capacitiva aplicada à expansão de sistemas elétricos**. Ph.D. Dissertation (Electric Engineering) — Universidade Federal de Minas Gerais, 2007.

CHIRAPONGSANANURAK, P.; SANTOSO, S.; DUGAN, R.; SMITH, J. Voltage regulation in distribution circuits with wind power. In: IEEE. **2012 IEEE Power and Energy Society General Meeting**. [S.l.], 2012. p. 1–8.

CHUA, L. O.; LIN, P. Y. **Computer-aided analysis of electronic circuits: Algorithms and computational techniques**. [S.l.]: Prentice Hall Professional Technical Reference, 1975.

CUPERTINO, A. F.; FARIAS, J. V. M.; PEREIRA, H. A.; SELEME, S. I.; TEODORESCU, R. Comparison of DSCC and SDBC modular multilevel converters for STATCOM application during negative sequence compensation. **IEEE Transactions on Industrial Electronics**, IEEE, 2018.

CUPERTINO, A. F.; FARIAS, J. V. M.; PEREIRA, H. A.; SELEME, S. I.; TEODORESCU, R. DSCC-MMC STATCOM main circuit parameters design considering positive and negative sequence compensation. **Journal of Control, Automation and Electrical Systems**, Springer, v. 29, n. 1, p. 62–74, 2018.

DARUS, R.; POU, J.; KONSTANTINOU, G.; CEBALLOS, S.; PICAS, R.; AGELIDIS, V. G. A modified voltage balancing algorithm for the modular multilevel converter: Evaluation for staircase and phase-disposition PWM. **IEEE transactions on power electronics**, IEEE, v. 30, n. 8, p. 4119–4127, 2014.

DAS, A.; NADEMI, H.; NORUM, L. A method for charging and discharging capacitors in modular multilevel converter. In: IEEE. **IECON 2011-37th Annual Conference on IEEE Industrial Electronics Society**. [S.l.], 2011. p. 1058–1062.

DEBNATH, S.; QIN, J.; BAHRANI, B.; SAEEDIFARD, M.; BARBOSA, P. Operation, control, and applications of the modular multilevel converter: A review. **IEEE transactions on power electronics**, IEEE, v. 30, n. 1, p. 37–53, 2015.

DU, S.; DEKKA, A.; WU, B.; ZARGARI, N. **Modular multilevel converters: analysis, control, and applications**. [S.l.]: John Wiley & Sons, 2018.

DUARTE, S. N. **Estratégias de Energização e Desenergização de um Compensador Estático Síncrono para Distribuição**. Tese (Dissertação de Mestrado) — Universidade Federal de Juiz de Fora, Juiz de Fora, Brasil, 2017.

DUARTE, S. N.; ALMEIDA, P. M.; BARBOSA, P. G. A novel energizing strategy for a grid-connected modular multilevel converter operating as static synchronous compensator. **International Journal of Electrical Power & Energy Systems**, Elsevier, v. 109, p. 672–684, 2019.

DUARTE, S. N.; ALMEIDA, P. M.; BARBOSA, P. G. Enhancing the performance of pre-charging strategy of a modular multilevel static synchronous compensator. **Journal of Control, Automation and Electrical Systems**, Springer, p. 1–11, 2020.

DUARTE, S. N.; FOGLI, G. A.; ALMEIDA, P. M.; BARBOSA, P. G. Energization and de-energization strategies of a DSTATCOM. **Brazilian Journal of Power Electronics**, SOBRAEP, v. 23, n. 1, p. 29–38, March 2018.

DUARTE, S. N.; GHETTI, F. T.; ALMEIDA, P. M. de; BARBOSA, P. G. Zero-sequence voltage compensation of a distribution network through a four-wire modular multilevel static synchronous compensator. **International Journal of Electrical Power & Energy Systems**, Elsevier, v. 109, p. 57–72, 2019.

DUARTE, S. N.; GHETTI, F. T.; ALMEIDA, P. M. de; BARBOSA, P. G. Experimental evaluation of negative-sequence voltage compensation in distribution networks by a modular multilevel static synchronous compensator. **Electric Power Systems Research**, Elsevier, v. 193, 2021.

DUARTE, S. N.; SOUZA, B. C.; ALMEIDA, P. M.; ARAUJO, L. R.; BARBOSA, P. G. Control algorithm for DSTATCOM to compensate consumer-generated negative and zero sequence voltage unbalance. **International Journal of Electrical Power & Energy Systems**, Elsevier, v. 120, p. 105957, 2020.

DUARTE, S. N.; SOUZA, B. C. de; ALMEIDA, P. M. de; ARAÚJO, L. R. de; BARBOSA, P. G. A compensation strategy based on consumer's voltage unbalance assessment for a distribution static synchronous compensator. **IEEE Latin America Transactions**, IEEE, v. 18, n. 01, p. 156–164, 2020.

FOGLI, G. A. **Controle de Conversor Multifuncional Aplicado a um Sistema de Geração Despachável Baseado em um Grupo Motor Gerador Diesel**. Tese (Tese de Doutorado) — Universidade Federal de Juiz de Fora, Juiz de Fora, Brasil, 2018.

FOGLI, G. A.; ALMEIDA, P. M. de; BARBOSA, P. G. Modelling and control of an interface power converter for the operation of small diesel gen-sets in grid-connected and stand-alone modes. **Electric Power Systems Research**, Elsevier, v. 150, p. 177–187, 2017.

FRANQUELO, L. G.; RODRIGUEZ, J.; LEON, J. I.; KOURO, S.; PORTILLO, R.; PRATS, M. A. The age of multilevel converters arrives. **IEEE industrial electronics magazine**, IEEE, v. 2, n. 2, p. 28–39, 2008.

FUCHS, E.; MASOUM, M. A. **Power quality in power systems and electrical machines**. 2^{nd}. [S.l.]: Academic Press, 2015. ISBN 9780128007822.

FURTADO, P.; RODRIGUES, M.; BRAGA, H.; BARBOSA, P. Two-phase three-wire shunt active power filter control by using the single-phase pq theory. v. 19, n. 3, p. 303–311, 2014.

GHETTI, F. T. **Aplicações de Conversores Multiníveis Modulares no Precessamento e Condicionamento da Energia Elétrica**. Tese (Tese de Doutorado) — Universidade Federal de Juiz de Fora, Juiz de Fora, Brasil, 2019.

GHETTI, F. T.; ALMEIDA, A. O.; ALMEIDA, P. M.; BARBOSA, P. G. Real time simulation of DC voltage equalization algorithms of a modular multilevel converter. **Brazilian Journal of Power Electronics**, SOBRAEP, v. 22, n. 4, p. 362–371, December 2017.

GHETTI, F. T.; FERREIRA, A. A.; BRAGA, H. A.; BARBOSA, P. G. A study of shunt active power filter based on modular multilevel converter (MMC). In: IEEE. **2012 10th IEEE/IAS International Conference on Industry Applications**. [S.l.], 2012. p. 1–6.

GREGORY, R. C. F.; SCOTTI, T. M.; OLIVEIRA, J. C. Evaluation of the methodologies for the allocation of imbalance accountability parcels. **Brazilian Symposium on Electrical Systems (SBSE)**, 2018.

GREGORY, R. C. F.; SCOTTI, T. M.; OLIVEIRA, J. C. de. Performance evaluation of unbalance sharing responsibility procedures. In: IEEE. **2018 Brazilian Symposium on Electrical Systems (SBSE)**. [S.l.], 2018. p. 1–6.

GYUGYI, L. **Solid-state synchronous voltage sources for dynamic compensation and real-time control of AC transmission lines**. [S.l.]: IEEE Standards Press, 1993.

GYUGYI, L. Dynamic compensation of AC transmission lines by solid-state synchronous voltage sources. **IEEE Transactions on Power Delivery**, IEEE, v. 9, n. 2, p. 904–911, 1994.

HAGIWARA, M.; AKAGI, H. Control and experiment of pulsewidth-modulated modular multilevel converters. **IEEE transactions on power electronics**, IEEE, v. 24, n. 7, p. 1737–1746, 2009.

HAN, C. **Power system dynamic voltage management with advanced STATCOM and energy storage system**. Tese (Ph.D. Thesis) — North Carolina State University, 2006.

HART, D. W. **Power electronics**. [S.l.]: Tata McGraw-Hill Education, 2011.

HINGORANI, N. G. Power electronics in electric utilities: role of power electronics in future power systems. **Proceedings of the IEEE**, IEEE, v. 76, n. 4, p. 481–482, 1988.

HINGORANI, N. G.; GYUGYI, L. **Understanding FACTS: concepts and technology of flexible AC transmission systems**. [S.l.]: IEEE press, 2000.

HINGORANI, N. G.; GYUGYI, L. **Understanding FACTS: Concepts and Technology of Flexible AC Transmission Systems**. [S.l.]: Wiley-IEEE Press, 2000.

IEC. **61000-3-13 - Electromagnetic compatibility (EMC) - limits - assessment of emission limits for the connection of unbalanced installations to MV, HV and EHV power systems**. [S.l.]: International Electrotechnical Commission, 2008.

IEEE 519-2014. **Recommended Practice and Requirements for Harmonic Control in Electric Power Systems**. 2014.

ISLAM, M. R.; GUO, Y.; ZHU, J. **Power converters for medium voltage networks**. [S.l.]: Springer, 2014.

JAYATUNGA, U.; PERERA, S.; CIUFO, P.; AGALGAONKAR, A. P. Deterministic methodologies for the quantification of voltage unbalance propagation in radial and interconnected networks. **IET Generation, Transmission & Distribution**, IET, v. 9, n. 11, p. 1069–1076, 2015.

JAYATUNGA, U.; PERERA, S.; CIUFO, P.; AGALGAONKAR, A. P. A refined general summation law for VU emission assessment in radial networks. **International Journal of Electrical Power & Energy Systems**, Elsevier, v. 73, p. 329–339, 2015.

JOUANNE, A. V.; BANERJEE, B. Assessment of voltage unbalance. **IEEE transactions on power delivery**, IEEE, v. 16, n. 4, p. 782–790, 2001.

KIM, J.-H.; LEE, Y.-S.; HAN, B.-m. New pre-charging scheme for MMC-based back-to-back HVDC system operated in nearest level control. In: IEEE. **Future Energy Electronics Conference and ECCE Asia (IFEEC 2017-ECCE Asia), 2017 IEEE 3rd International**. [S.l.], 2017. p. 1445–1450.

LARSSON, T.; THORVALDSSON, B.; AKESSON, B. **Device for energizing a voltage-source converter**. [S.l.]: Google Patents, 2002. US Patent 6,337,802.

LESNICAR, A.; MARQUARDT, R. An innovative modular multilevel converter topology suitable for a wide power range. In: IEEE. **Power Tech Conference Proceedings, 2003 IEEE Bologna**. [S.l.], 2003. v. 3, p. 6–pp.

LESNICAR, A.; MARQUARDT, R. New concept for high voltage modular multilevel converter. In: **PESC 2004 Conference in Aachen**. [S.l.: s.n.], 2004.

LI, B.; XU, D.; ZHANG, Y.; YANG, R.; WANG, G.; WANG, W.; XU, D. Closed-loop precharge control of modular multilevel converters during start-up processes. **IEEE Transactions on Power Electronics**, IEEE, v. 30, n. 2, p. 524–531, 2015.

LI, B.; ZHANG, Y.; XU, D.; YANG, R. Start-up control with constant precharge current for the modular multilevel converter. In: IEEE. **Industrial Electronics (ISIE), 2014 IEEE 23rd International Symposium on**. [S.l.], 2014. p. 673–676.

LI, C.; DAI, K.; LIN, D.; XU, C.; CHEN, C.; DAI, Z. Independent positive- and negative-sequence control for MMC-SAPF with unbalanced PCC voltage. In: IEEE. **Energy Conversion Congress and Exposition (ECCE), 2017 IEEE**. [S.l.], 2017. p. 1823–1829.

LI, J.; KONSTANTINOU, G.; WICKRAMASINGHE, H. R.; POU, J. Operation and control methods of modular multilevel converters in unbalanced AC grids: A review. **IEEE Journal of Emerging and Selected Topics in Power Electronics**, IEEE, 2018.

LI, K.; ZHAO, C. New technologies of modular multilevel converter for VSC-HVDC application. In: IEEE. **Power and Energy Engineering Conference (APPEEC), 2010 Asia-Pacific**. [S.l.], 2010. p. 1–4.

LI, Z.; WANG, P.; CHU, Z.; ZHU, H.; LUO, Y.; LI, Y. An inner current suppressing method for modular multilevel converters. **IEEE Transactions on Power Electronics**, IEEE, v. 28, n. 11, p. 4873–4879, 2013.

LIU, W.; LI, G.; UGALDE-LOO, C. E.; LIANG, J. Start-up strategy for modular multilevel converters with modified nearest level modulation method. In: **8th Renewable Power Generation Conference (RPG 2019)**. [S.l.]: IET, 2019. p. 1–6. ISBN 978-1-83953-125-5.

LIU, W.; LI, K.-J.; LIU, Z.; WANG, M. A simple and novel precharging control strategy for modular multilevel converter. **IEEE Access**, IEEE, v. 7, p. 170500–170512, 2019.

LIU, Z.; LU, J.; OU, Z.; MA, M.; YUAN, C.; XIAO, X.; WANG, H. The start control strategy design of unified power quality conditioner based on modular multilevel converter. In: IEEE. **Electric Machines & Drives Conference (IEMDC), 2013 IEEE International**. [S.l.], 2013. p. 933–937.

Long, B.; Cao, T.; Fang, W.; KIL, T. C.; Guerrero, J. M. Model predictive control of a three-phase two-level four-leg grid-connected converter based on sphere decoding method. **IEEE Transactions on Power Electronics**, p. 1–1, 2020.

LUDOIS, D. C.; VENKATARAMANAN, G. Simplified terminal behavioral model for a modular multilevel converter. **IEEE Transactions on Power Electronics**, IEEE, v. 29, n. 4, p. 1622–1631, 2014.

MALINOWSKI, M.; GOPAKUMAR, K.; RODRIGUEZ, J.; PÉREZ, M. A. A survey on cascaded multilevel inverters. **IEEE Transactions on Industrial Electronics**, IEEE, v. 57, n. 7, p. 2197–2206, 2010.

MANOLAROU, M.; KOSTAKIS, G.; MANIAS, S. Inrush current limiting technique for low-voltage synchronous DC/DC converters. **IEE Proceedings-Electric Power Applications**, IET, v. 152, n. 5, p. 1179–1183, 2005.

MEERSMAN, B.; RENDERS, B.; DEGROOTE, L.; VANDOORN, T.; VANDEVELDE, L. Control design of grid-connected three-phase inverters for voltage unbalance correction. In: IEEE. **Universities Power Engineering Conference (UPEC), 2009 Proceedings of the 44th International**. [S.l.], 2009. p. 1–5.

MIHALIC, R.; EREMIA, M.; BLAZIC, B. Static synchronous compensator–Statcom. **Advanced Solutions in Power Systems: HVDC, FACTS, and Artificial Intelligence**, Wiley Online Library, p. 459–525, 2016.

MILLER, T. J. E. **Reactive power control in electric systems**. [S.l.]: Wiley, 1982.

MOHAN, N.; UNDELAND, T. M. **Power electronics: Converters, applications, and design**. [S.l.]: John Wiley & Sons, 2007.

MONTEIRO, H. L. M. **Impedance Estimation Method by Using Injection of Controlled Signals**. Tese (Ph.D. Thesis) — Federal University of Juiz de Fora, Juiz de Fora, Brazil, 2018.

MORI, S.; MATSUNO, K.; HASEGAWA, T.; OHNISHI, S.; TAKEDA, M.; SETO, M.; MURAKAMI, S.; ISHIGURO, F. Development of a large static var generator using self-commutated inverters for improving power system stability. **IEEE Transactions on Power Systems**, IEEE, v. 8, n. 1, p. 371–377, 1993.

NEMA Standards Publication MG 1-2016. **Motors and Generators**. [S.l.]: National Electrical Manufacturers Association, 2016.

OGHORADA, O.; ZHANG, L. Analysis of star and delta connected modular multilevel cascaded converter-based STATCOM for load unbalanced compensation. **International Journal of Electrical Power & Energy Systems**, Elsevier, v. 95, p. 341–352, 2018.

ORCAJO, G. A. A.; DIEZ, J. R.; CANO, J. M.; NORNIELLA, J. G.; GONZÁLEZ, J. F. P.; ROJAS, C. H.; ARDURA, P.; CIFRIÁN, D. Enhancement of power quality in an actual hot rolling mill plant through a STATCOM. **IEEE Transactions on Industry Applications**, IEEE, v. 56, n. 3, p. 3238–3249, 2020.

PETRY, C. A. Metodologia de projeto de retificadores com filtro capacitivo. **Revista Ilha Digital**, v. 3, p. 77–85, 2012.

PILLAY, P.; MANYAGE, M. Definitions of voltage unbalance. **IEEE Power Engineering Review**, v. 21, n. 5, p. 50–51, 2001.

PINTO, R. L. **Aplicação de um sistema especialista fuzzy para redução de manobras de dispositivos shunts chaveados automaticamente por um compensador estático**. Master Thesis(Electric Engineering) — Universidade Federal do Rio de Janeiro, 2010.

PRIETO-ARAUJO, E.; JUNYENT-FERRÉ, A.; CLARIANA-COLET, G.; GOMIS-BELLMUNT, O. Control of modular multilevel converters under singular unbalanced voltage conditions with equal positive and negative sequence components. **IEEE Transactions on Power Systems**, IEEE, v. 32, n. 3, p. 2131–2141, 2017.

PUTRUS, G.; SUWANAPINGKARL, P.; JOHNSTON, D.; BENTLEY, E.; NARAYANA, M. Impact of electric vehicles on power distribution networks. In: IEEE. **Vehicle Power and Propulsion Conference, 2009. VPPC'09. IEEE**. [S.l.], 2009. p. 827–831.

RASHID, M. H. **Power electronics handbook**. [S.l.]: Butterworth-Heinemann, 2017.

RIBEIRO, R. L.; SOUSA, R. M.; JR., E. C. S.; ROCHA, T. O. Enhanced power quality compensation of shunt active power filters without harmonic detection schemes. **Brazilian Journal of Power Electronics**, SOBRAEP, v. 19, n. 4, p. 332–342, 2014.

ROCHA, A. C.; ARAÚJO, A. E. A. de; NOVAIS, M. dos S. Manobra de bancos de capacitores – resultados práticos da aplicação de técnicas de mitigação de transitórios. In: **V SBQEE (Seminário Brasileiro sobre Qualidade de Energia Elétrica)**. [S.l.: s.n.], 2003.

RODRIGUES, M. C.; SOUZA, I. D.; FERREIRA, A. A.; BARBOSA, P. G.; BRAGA, H. A. Simultaneous active power filter and G2V (or V2G) operation of EV on-board power electronics. In: IEEE. **IECON 2013-39th Annual Conference of the IEEE Industrial Electronics Society**. [S.l.], 2013. p. 4684–4689.

RODRIGUEZ, J.; LAI, J.-S.; PENG, F. Z. Multilevel inverters: A survey of topologies, controls, and applications. **IEEE Transactions on Industrial Electronics**, IEEE, v. 49, n. 4, p. 724–738, 2002.

RODRIGUEZ, P.; TEODORESCU, R.; CANDELA, I.; TIMBUS, A. V.; LISERRE, M.; BLAABJERG, F. New positive-sequence voltage detector for grid synchronization of power converters under faulty grid conditions. In: IEEE. **37th IEEE Power Electronics Specialists Conference (PESC'06)**. [S.l.], 2006. p. 1–7.

RUIZ-RODRIGUEZ, F.; HERNÁNDEZ, J.; JURADO, F. Voltage unbalance assessment in secondary radial distribution networks with single-phase photovoltaic systems. **International Journal of Electrical Power & Energy Systems**, Elsevier, v. 64, p. 646–654, 2015.

SAEEDIFARD, M.; IRAVANI, R. Dynamic performance of a modular multilevel back-to-back HVDC system. **IEEE Transactions on power delivery**, IEEE, v. 25, n. 4, p. 2903–2912, 2010.

SALLAM, A. A.; MALIK, O. P. **Electric distribution systems**. [S.l.]: Wiley-IEEE Press, 2018.

SCHAUDER, C.; GERNHARDT, M.; STACEY, E.; LEMAK, T.; GYUGYI, L.; CEASE, T.; EDRIS, A. Development of a ±100 Mvar static condenser for voltage control of transmission systems. **IEEE Transactions on Power Delivery**, IEEE, v. 10, n. 3, p. 1486–1496, 1995.

SEIPHETLHO, T.; RENS, A. On the assessment of voltage unbalance. In: IEEE. **Proceedings of 14th International Conference on Harmonics and Quality of Power-ICHQP 2010**. [S.l.], 2010. p. 1–6.

SHARIFABADI, K.; HARNEFORS, L.; NEE, H.-P.; NORRGA, S.; TEODORESCU, R. **Design, control, and application of modular multilevel converters for HVDC transmission systems**. [S.l.]: John Wiley & Sons, 2016.

SHARKH, S. M.; ABU-SARA, M. A.; ORFANOUDAKIS, G. I.; HUSSAIN, B. **Power electronic converters for microgrids**. [S.l.]: John Wiley & Sons, 2014.

SHI, K.; SHEN, F.; LV, D.; LIN, P.; CHEN, M.; XU, D. A novel start-up scheme for modular multilevel converter. In: IEEE. **Energy Conversion Congress and Exposition (ECCE), 2012 IEEE**. [S.l.], 2012. p. 4180–4187.

SHI, X.; LIU, B.; WANG, Z.; LI, Y.; TOLBERT, L. M.; WANG, F. Modeling, control design, and analysis of a startup scheme for modular multilevel converters. **IEEE Transactions on Industrial Electronics**, IEEE, v. 62, n. 11, p. 7009–7024, 2015.

SHOJAIE, M.; MOKHTARI, H. A method for determination of harmonics responsibilities at the point of common coupling using data correlation analysis. **IET Generation, Transmission & Distribution**, IET, v. 8, n. 1, p. 142–150, 2014.

SINGH, B.; CHANDRA, A.; AL-HADDAD, K. **Power quality: problems and mitigation techniques**. [S.l.]: John Wiley & Sons, 2015.

SINGH, B.; JAYAPRAKASH, P.; KOTHARI, D. A T-connected transformer and three-leg VSC based DSTATCOM for power quality improvement. **IEEE Transactions on Power Electronics**, IEEE, v. 23, n. 6, p. 2710–2718, 2008.

SONG, Y.-H.; JOHNS, A. **Flexible ac transmission systems (FACTS)**. [S.l.]: IET, 1999.

SRINIVASAN, K.; JUTRAS, R. Conforming and non-conforming current for attributing steady state power quality problems. **IEEE Transactions on Power Delivery**, IEEE, v. 13, n. 1, p. 212–217, 1998.

SUN, Y.; LI, P.; LI, S.; ZHANG, L. Contribution determination for multiple unbalanced sources at the point of common coupling. **Energies**, Multidisciplinary Digital Publishing Institute, v. 10, n. 2, p. 171, 2017.

SUN, Y.; XIE, X.; LI, P. Unbalanced source identification at the point of evaluation in the distribution power systems. **International Transactions on Electrical Energy Systems**, Wiley Online Library, v. 28, n. 1, p. e2460, 2018.

TIAN, K.; WU, B.; DU, S.; XU, D. D.; CHENG, Z.; ZARGARI, N. R. A simple and cost-effective precharge method for modular multilevel converters by using a low-voltage DC source. **IEEE Transactions on Power Electronics**, IEEE, v. 31, n. 7, p. 5321–5329, 2016.

TSOLARIDIS, G.; KONTOS, E.; PARIKH, H.; SANCHEZ-LOECHES, R.; TEODORESCU, R.; CHAUDHARY, S. K. Control of a modular multilevel converter STATCOM under internal and external unbalances. In: IEEE. **IECON 2016-42nd Annual Conference of the IEEE Industrial Electronics Society**. [S.l.], 2016. p. 6494–6499.

TU, Q.; XU, Z.; XU, L. Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters. **IEEE transactions on power delivery**, IEEE, v. 26, n. 3, p. 2009–2017, 2011.

VIJAY, A.; DOOLLA, S.; CHANDORKAR, M. C. Unbalance mitigation strategies in microgrids. **IET Power Electronics**, IET, 2020.

WANG, F.; MAO, H.; XU, D.; RUAN, Y. Negative-sequence admittance control scheme for distributed compensation of grid voltage unbalance. In: IEEE. **2012 IEEE 13th Workshop on Control and Modeling for Power Electronics (COMPEL)**. [S.l.], 2012. p. 1–8.

WANG, J.; TANG, Y.; QI, Y.; LIN, P.; ZHANG, Z. A unified startup strategy for modular multilevel converters with deadbeat predictive current control. **IEEE Transactions on Industrial Electronics**, IEEE, 2020.

WATANABE, E. H.; LIMA, F. K. d.; DIAS, R. F. daSilva; AREDES, M.; BARBOSA, P. G.; BARCELOS, S. L. L.; JR, G. S. Flexible ac transmission systems. In: **Power Electronics Handbook**. [S.l.]: Elsevier, 2018. p. 885–909.

XU, C.; DAI, K.; CHEN, X.; KANG, Y. Unbalanced PCC voltage regulation with positive-and negative-sequence compensation tactics for MMC-DSTATCOM. **IET Power Electronics**, IET, v. 9, n. 15, p. 2846–2858, 2016.

XU, J.; ZHAO, C.; ZHANG, B.; LU, L. New precharge and submodule capacitor voltage balancing topologies of modular multilevel converter for VSC-HVDC application. In: IEEE. **Power and Energy Engineering Conference (APPEEC), 2011 Asia-Pacific**. [S.l.], 2011. p. 1–4.

XU, W.; LIU, Y. A method for determining customer and utility harmonic contributions at the point of common coupling. **IEEE Transactions on Power Delivery**, IEEE, v. 15, n. 2, p. 804–811, 2000.

XU, Z.; XIAO, H.; ZHANG, Z. Selection methods of main circuit parameters for modular multilevel converters. **IET Renewable Power Generation**, IET, v. 10, n. 6, p. 788–797, 2016.

XUE, Y.; XU, Z.; TANG, G. Self-start control with grouping sequentially precharge for the C-MMC-based HVDC system. **IEEE Transactions on Power delivery**, IEEE, v. 29, n. 1, p. 187–198, 2014.

YAN, R.; LI, Y.; SAHA, T. K.; WANG, L.; HOSSAIN, M. I. Modeling and analysis of open-delta step voltage regulators for unbalanced distribution network with photovoltaic power generation. **IEEE Transactions on Smart Grid**, IEEE, v. 9, n. 3, p. 2224–2234, 2018.

YANG, Y.; GE, Q.; LEI, M.; WANG, X.; YANG, X.; GOU, R. Pre-charging control strategies of modular multilevel converter. In: IEEE. **Electrical Machines and Systems (ICEMS), 2013 International Conference on**. [S.l.], 2013. p. 1842–1845.

YANG, Y.; WANG, Y.; MA, X. Determining the responsibility of three-phase unbalanced sources based on RICA. **Energies**, Multidisciplinary Digital Publishing Institute, v. 12, n. 15, p. 2849, 2019.

YAZDANI, A.; IRAVANI, R. **Voltage-sourced converters in power systems: Modeling, control, and applications**. [S.l.]: John Wiley & Sons, 2010.

ZHANG, L.; QIN, J.; WU, X.; DEBNATH, S.; SAEEDIFARD, M. A generalized precharging strategy for soft startup process of the modular multilevel converter-based HVDC systems. **IEEE Transactions on Industry Applications**, IEEE, v. 53, n. 6, p. 5645–5657, 2017.

ZYGMANOWSKI, M.; GRZESIK, B.; NALEPA, R. Capacitance and inductance selection of the modular multilevel converter. In: IEEE. **Power Electronics and Applications (EPE), 2013 15th European Conference on**. [S.l.], 2013. p. 1–10.

APPENDIX A – Parameters of the 24 kV electric network and the MMC-STATCOM with 14 SMs per leg

This appendix presents the parameters of the electric network, MMC-STATCOM and digital filters used in Chapter 2, Chapter 3 and Chapter 4. Moreover, considerations on the MMC-STATCOM parameters are also presented.

Tables 8, 9 and 10 show the parameters of the 24 kV electric network, MMC-STATCOM with 14 SMs per arm and digital filters, respectively, considering 100 MVA as base power.

Table 8 – Parameters of the 24 kV electric network.

Parameter	Value
Rated RMS line-to-line voltage (V_s)	24 kV
Fundamental frequency (f_s)	50 Hz
Short-circuit power	200 MVA
X/R ratio	6

Source: Elaborated by the author (2021).

Table 9 – Parameters of the MMC-STATCOM with 14 SMs per arm.

Parameter	Value
Rated power	10 MVA
DC terminal voltage (V_{dc}^*)	50 kV
Submodule DC voltage (V_C)	3.57 kV
Submodule capacitance (C)	1800 μF
Number of submodules per arm (n)	14
Inductance of the passive filters (L_f and L_i)	19.7 mH
Resistance of the passive filters (R_f and R_i)	0.31 Ω
Series resistance of the DC capacitors (R_C)	31 mΩ
Conduction resistance of the IGBTs (R_{igbt})	0.18 mΩ
Diode resistances of the IGBTs (R_D)	0.18 mΩ
Switching frequency (f_{sw})	1.2 kHz

Source: Elaborated by the author (2021).

Table 10 – Parameters of the digital filters of the MMC-STATCOM with 14 SMs per arm.

Parameters	Value
Gain of the SOGI (k)	4.2
Resonant frequency of the filter F_n (ω_o)	628.3 rad/s
Quality factor of the filter F_n (Q)	0.5

Source: Elaborated by the author (2021).

The MMC-STATCOM arm inductances must be carefully chosen to avoid resonance with the DC capacitors of the SMs (CUPERTINO *et al.*, 2018b; XU; XIAO; ZHANG,

2016). In addition, this inductance should ensure a cut-off frequency at least one decade below the switching frequency of the static compensator. Thus, based on the electric network parameters of Table 8, the value of the MMC-STATCOM's filter inductances was chosen to be approximately 0.1 pu (SHARIFABADI *et al.*, 2016).

On the other hand, the SM capacitance of a MMC-STATCOM must be designed to ensure the stable operation of the compensator connected to an unbalanced network. Thus, assuming 40 kJ/MVA for the energy-power ratio of the MMC-STATCOM, the minimum value of the capacitance for the SMs is 0.75 mF (CUPERTINO *et al.*, 2018b; XU; XIAO; ZHANG, 2016; ZYGMANOWSKI; GRZESIK; NALEPA, 2013). However, the DC capacitance of each SM was chosen to be higher than twice the minimum value.

Considering a maximum voltage of 3.6 kV recommended for a commercial IGBT of 6.5 kV rated voltage (ISLAM; GUO; ZHU, 2014), and that the DC terminal voltage of the MMC-STATCOM is 50 kV, one can design the MMC-STATCOM with 14 SMs per arm. Thus, the voltage across each semiconductor of the SM bridges will be 3.57 kV (= 50 kV/14). Since the MMC-STATCOM has $n = 14$ SMs per arm it is possible to synthesize voltages with $(2n + 1) = 29$ levels at the output terminals.

APPENDIX B – Parameters of the 4.16 kV electric network and the MMC-STATCOM with 3 SMs per arm

This appendix presents the parameters of the electric network and MMC-STATCOM used in the digital simulations of the Chapter 5.

Tables 11 and 12 show the parameters of the 4.16 kV electric network and the MMC-STATCOM with 3 SMs per arm, respectively.

Table 11 – Parameters of the 4.16 kV electric network.

Parameter	Value
Rated RMS line-to-line voltage (V_s)	4.16 kV
Fundamental frequency (f_s)	60 Hz
Equivalent resistances seen from bus 670 (R_{s1} and R_{s2})	0.35 Ω
Equivalent inductances seen from bus 670 (L_{s1} and L_{s2})	2.08 mH
Equivalent resistances seen from bus 670 (R_{s0})	1.47 Ω
Equivalent inductances seen from bus 670 (L_{s0})	4.84 mH

Source: Elaborated by the author (2021).

Table 12 – Parameters of the MMC-STATCOM with 3 SMs per arm.

Parameter	Value
DC terminal voltage (V_{dc}^*)	8.8 kV
Submodule DC voltage (V_C)	2.93 kV
Submodule capacitance (C)	540 µF
Number of submodules per arm	3
Inductance of the passive filters (L_f and L_i)	9.77 mH
Resistance of the passive filters (R_f and R_i)	185 mΩ
Switching frequency (f_{sw})	1.44 kHz

Source: Elaborated by the author (2021).

Tables 13 and 14 show the parameters of the digital filters and the controller gains of the MMC-STATCOM with 3 SMs per arm, respectively.

Table 13 – Parameters of the digital filters of the MMC-STATCOM with 3 SMs per arm.

Parameter	Value
Gain of the SOGI (k)	4.2
Resonant frequency of the filter F_n (ω_o)	754 rad/s
Quality factor of the filter F_n (Q)	0.5

Source: Elaborated by the author (2021).

The parameters of the loads, capacitor bank and feeders of the 4.16 kV 5-bus system of Diagram 34 are given in Tables 15, 16 and 17, respectively.

Table 14 – Controller gains of the MMC-STATCOM with 3 SMs per arm.

Controller	**Gain**	**Value**
$K_{i1}(s)$	$k_{p,i1}$	19.54 V/A
	$k_{i,i1}$	370 V/(A s)
$K_{v1}(s)$	k_{v1}	63.71 A/(V s)
$K_{i2}(s)$	$k_{p,i2}$	19.54 V/A
	$k_{i,i2}$	370 V/(A s)
$K_{v2}(s)$	k_{v2}	63.71 A/(V s)
$K_{vdc}(s)$	$k_{p,vdc}$	7.06 µA/V^2
	$k_{i,vdc}$	0.18 mA/(V^2 s)
$K_{cir}(s)$	$k_{p,cir}$	3.3 V/A
	$k_{i,cir}$	313 V/(A s)

Source: Elaborated by the author (2021).

Table 15 – Load parameters of the 4.16 kV 5-bus system.

Bus	**Phase**	**P (kW)**	**Q (kvar)**
671	A	110.3	71.9
671	B	133.3	86.7
671	C	166.7	108.3
633	A	371.8	214.5
633	B	220.0	100.0
633	C	184.8	84.7
670	A	760.0	430.0
670	B	623.7	454.3
670	C	863.6	495.3

Source: Elaborated by the author (2021).

Table 16 – Capacitor bank parameters of the 4.16 kV 5-bus system.

Bus	**Phase**	**Q (kvar)**	**V (kV)**
632	3ϕ	4600	4.16

Source: Elaborated by the author (2021).

Table 17 – Feeder parameters of the 4.16 kV 5-bus system.

Parameter	**Feeder**			
	650-632	632-670	632-633	632-671
Length (mi)	0.76	0.70	0.19	0.78
R_{aa} (Ω/mi)	0.3465	0.3465	0.7526	0.7526
R_{ab} (Ω/mi)	0.1560	0.1560	0.1580	0.1580
R_{bb} (Ω/mi)	0.3375	0.3375	0.7475	0.7475
R_{ac} (Ω/mi)	0.1580	0.1580	0.1560	0.1560
R_{bc} (Ω/mi)	0.1535	0.1535	0.1535	0.1535
R_{cc} (Ω/mi)	0.3414	0.3414	0.7436	0.7436
X_{aa} (Ω/mi)	1.0179	1.0179	1.1814	1.1814
X_{ab} (Ω/mi)	0.5017	0.5017	0.4236	0.4236
X_{bb} (Ω/mi)	1.0478	1.0478	1.1983	1.1983
X_{ac} (Ω/mi)	0.4236	0.4236	0.5017	0.5017
X_{bc} (Ω/mi)	0.3849	0.3849	0.3849	0.3849
X_{cc} (Ω/mi)	1.0348	1.0348	1.2112	1.2112

Source: Elaborated by the author (2021).

APPENDIX C – PWL approximation

Tables 18 and 19 show the values of the breaking points and coefficients of the PWL approximations of Figures 7 and 8, respectively.

Table 18 – Coefficients of the PWL approximation of Figure 7.

Breaking points			**Coefficients**
k	$V_{dc,k}$ (kV)	α_k (°)	
Initial	0	162.93	$b = -0.01321966730$
1	5.5	153.34	$c_1 = -0.0000437369$
2	10	145.10	$c_2 = -0.0000631743$
3	14	137.27	$c_3 = -0.0000870663$
4	17.5	129.81	$c_4 = -0.0001161347$
5	20.5	122.72	$c_5 = -0.0001522574$
6	23	116.05	$c_6 = -0.0001958304$
7	25	109.93	$c_7 = -0.0002416113$
8	26.5	104.61	$c_8 = -0.0002692124$
9	27.5	100.53	$c_9 = -0.0003407905$
10	28.5	95.77	$c_{10} = -0.0004079319$
11	29.05	92.70	$c_{11} = -0.0004077203$
12	29.5	89.82	$c_{12} = -0.0005557281$
13	29.94	86.52	$c_{13} = -0.0008186980$
14	30.3	83.23	$c_{14} = -0.0012435170$
15	30.6	79.74	$c_{15} = -0.0019311702$
16	30.8	76.64	$c_{16} = -0.0046013631$
Final	31	71.70	$a = 500.101773325$

Source: Elaborated by the author (2021).

Table 19 – Coefficients of the PWL approximation of Figure 8.

Breaking points			**Coefficients**
k	$V_{dc,k}$ (kV)	α_k (°)	
Initial	0	161.52	$b = -0.00914142992$
1	12	139.73	$c_1 = -0.0001854914$
2	19.9	122.46	$c_2 = 0.004233629200$
3	20.1	123.71	$c_3 = -0.0046011221$
4	26	106.47	$c_4 = -0.0007407894$
5	28.8	94.14	$c_5 = -0.0014374548$
6	30.3	83.23	$c_6 = -0.0045942874$
Final	31	71.70	$a = 3.718534136170$

Source: Elaborated by the author (2021).

APPENDIX D – The Park transform

This appendix presents the Park transform used to control the MMC-STATCOM in the synchronous reference frame.

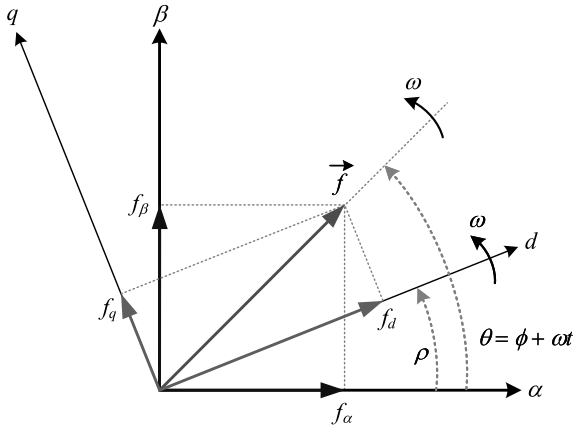
Figure 69 depicts the $\alpha\beta \rightarrow dq$ transformation, where f is a function of the time, f_α and f_β are the components in the $\alpha\beta$ stationary reference frame, and f_d and f_q are the components in the synchronous reference frame. These quantities are related to each other by:

$$\begin{bmatrix} f_\alpha \\ f_\beta \end{bmatrix} = \begin{bmatrix} \cos\rho & -\sin\rho \\ \sin\rho & \cos\rho \end{bmatrix} \begin{bmatrix} f_d \\ f_q \end{bmatrix} \tag{D.1}$$

and

$$\begin{bmatrix} f_d \\ f_q \end{bmatrix} = \begin{bmatrix} \cos\rho & \sin\rho \\ -\sin\rho & \cos\rho \end{bmatrix} \begin{bmatrix} f_\alpha \\ f_\beta \end{bmatrix}. \tag{D.2}$$

Figure 69 – Spatial representation of $\alpha\beta$ to dq transformation.



Source: Reproduced from (DUARTE *et al.*, 2019).